Features

STC8H1K08TR-36I-TSSOP20/QFN20(Touch key/RTC family)

1. Features and Price(Quasi 16-bit MCU with 16-bit hardware multiplier and divider MDU16)

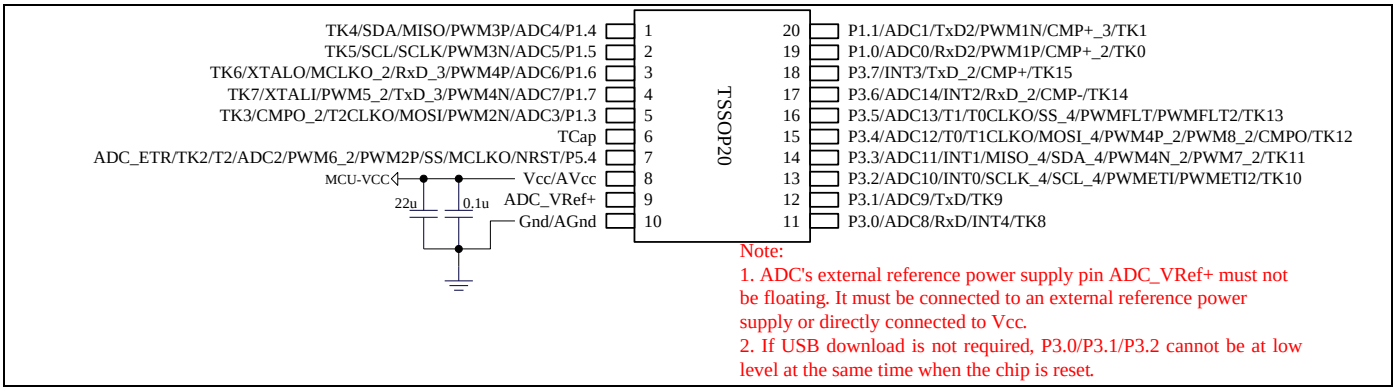
➢ **Selection and price (No external crystal and external reset required with 15 channels 12-bit ADC)**

MCU	Operating voltage（V）	Flash Code Memory (100 thousand times) (Byte)	idata Internal DATA RAM(Byte)	xdata Internal extended SRAM (Byte)	Enhanced Dual DPTR increasing or decreasing	EEPROM 100 thousand times) (Byte)	Interrupt(INT0/INT1/INT2/INT3/INT4) (can Maximum I/O Lines	Traditional I/O	All I/O ports support interrupts and can wake	DMA UARTs which can wake-up CPU	Touch key	RTC	DMA SPI which can wake-up CPU	I²C which can wake-up CPU	MDU16 (Hardware 16-bit Multiplier and Divider)	Timers/Counters (T0-T4 Pin can wake-up CPU)	16-bit advanced PWM timer with	Power-down Wake-up timer	DMA 15 channels high speed ADC (8 PWMs can be used as 8 DACs)	Comparator (May be used as ADC to detect	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 levels optional reset threshold voltage	Internal high precision Clock (adjustbal under 36MHz)	Clock output and Reset	Password can be set for next update	Program encrypted transmission (Anti-blocking)	Support RS485 download	Support software USB download directly	Online debug itself	Price & Package		products supply information
																														TSSOP20	QFN20	
STC8H1K08TR	1.9-5.5	8K	256	1K	2	4K	16	Y	Y	2	Y	Y	Y	Y	Y	3	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	¥2	¥2	Some available
STC8H1K17TR	1.9-5.5	17K	256	1K	2	IAP	16	Y	Y	2	Y	Y	Y	Y	Y	3	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√	√	

- **Core**
  - ✓ Ultra-high speed 8051 Core with single clock per machine cycle, which is called 1T and the speed is about 12 times faster than traditional 8051
  - ✓ Fully compatible instruction set with traditional 8051
  - ✓ 29 interrupt sources and 4 interrupt priority levels
  - ✓ Online debugging is supported
- **Operating voltage**
  - ✓ 1.9V～5.5V
- **Operating temperature**
  - ✓ -40℃~85℃(The chip is produced in -40℃～125℃ process. Please refer to the description of the electrical characteristics chapter for applications beyond the temperature range)
- **Flash memory**
  - ✓ Up to 17Kbytes of Flash memory to be used for storing user code
  - ✓ Configurable EEPROM size, 512bytes single page for being erased, which can be repeatedly erased more than 100 thousand times.
  - ✓ In-System-Programming, ISP in short, can be used to update the application code. No special programmer is needed.
  - ✓ Online debugging with single chip is supported, and no special emulator is needed. The number of breakpoints is unlimited theoratically.
- **SRAM**
  - ✓ 128 bytes internal direct access RAM (DATA, use keyword *data* to declare in C language program)
  - ✓ 128 bytes internal indirect access RAM (IDATA, use keyword *idata* to declare in C language program)
  - ✓ 1024 bytes internal extended RAM (internal XDATA, use keyword *xdata* to declare in C language program)
- **Clock**
  - ✓ Internal high precise RC clock IRC(IRC for short, ranges from 4MHz to 36MHz), adjustable while ISP and can be divided to lower frequency by user software, 100KHz for instance.
    - ✓ Error:±0.3% (at the temperature 25℃)
    - ✓ -1.35%～+1.30% temperature drift (at the temperature range of -40℃ to +85℃)
    - ✓ -0.76%～+0.98% temperature drift (at the temperature range of -20℃ to 65℃)
  - ✓ Internal 32KHz low speed IRC with large error
  - ✓ External crystal (4MHz～33MHz) and external clock
    Users can freely choose the above 3 clock sources
- **Reset**
  - ✓ Hardware reset
    - ✓ Power-on reset. Measured voltage is 1.69V~1.82V. (Effective when the chip does not enable the low voltage reset function)
      The power-on reset voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of the power-on reset, the chip is in a reset state; when the voltage rises from 0V to the upper threshold voltage of power-on reset, the chip is released from the reset state.
    - ✓ Reset by reset pin. The default function of P5.4 is the I/O port. The P5.4 pin can be set as the reset pin while ISP download. (Note: When the P5.4 pin is set as the reset pin, the reset level is low.)
    - ✓ Watch dog timer reset
    - ✓ Low voltage detection reset. 4 low voltage detection levels are provided, 1.9V, 2.3V, 2.8V, 3.0V. Each level of low-voltage detection voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of low-voltage detection, the low-voltage detection takes effect. When the voltage rises from 0V to the upper threshold voltage, the low voltage detection becomes effective.
  - ✓ Software reset
    - ✓ Writing the reset trigger register using software
- **Interrupts**
  - ✓ 29 interrupt sources: INT0(Supports rising edge and falling edge interrupt), INT1(Supports rising edge and falling edge interrupt), INT2(Supports falling edge interrupt only), INT3(Supports falling edge interrupt only), INT4(Supports falling edge interrupt only), timer 0, timer 1, timer 2, UART 1, UART 2, ADC, LVD, SPI, I^2C, comparator, PWMA, PWMB, RTC, TKS, P1, P3, P5, DMA receive and transmit interrupts of UART 1, DMA receive and transmit interrupts of UART 2, DMA interrupt of SPI, DMA interrupt of ADC and DMA interrupt of memory-to-memory.
  - ✓ 4 interrupt priority levels
  - ✓ Interrupts that can wake up the CPU in clock stop mode: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), RXD(P3.0/P3.6/P1.6), RXD2(P1.0), I2C_SDA(P1.4/P3.3), SPI_SS(P5.4/P3.5), Comparator interrupt, LVD interrupt, Power-down wake-up timer and interrupts of all I/O ports.

- **Digital peripherals**
  - ✓ 3 16-bit timers: timer0, timer1, timer2, where the mode 3 of timer 0 has the Non-Maskable Interrupt (NMI in short) function. Mode 0 of timer 0 and timer 1 is 16-bit Auto-reload mode.
  - ✓ 2 high speed UARTs: UART1, UART2, whose maximum baudrate clock may be FOSC/4
  - ✓ 8 channels/2 groups of enhanced PWM, which can realize control signals with dead time, and support external fault detection function. In addition, supports 16-bit timers, 8 external interrupts, 8 external captures and pulse width measurement functions.
  - ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
  - ✓ I^2C: Master mode or slave mode are supported.
  - ✓ MDU16: Hardware 16-bit Multiplier and Divider which supports 32-bit divided by 16-bit, 16-bit divided by 16-bit, 16-bit multiplied by 16-bit, data shift, and data normalization operations.
  - ✓ RTC: Support year, month, day, hour, minute, second, sub-second (1/128 second). And supports clock interrupt and a set of alarm clocks (Note: A version of the chip does not have this function)
  - ✓ I/O port interrupt: All I/Os support interrupts, each group of I/O interrupts has an independent interrupt entry address, all I/O interrupts can support 4 types interrupt mode: high level interrupt, low level interrupt, rising edge interrupt, falling edge interrupt. Provides 4 levels of interrupt priority and supports power-down wake-up function.
  - ✓ DMA: support Memory-To-Memory, SPI, UART1TX/UART1RX, UART2TX/UART2RX, ADC(Automatically calculates the average of multiple ADC results)
- **Analog peripherals**
  - ✓ Ultra high speed ADC which supports 12-bit precision 15 channels (channel 0 to channel 14) analog-to-digital conversion. The maximum speed can be 800K(800K ADC conversions per second)
  - ✓ ADC channel 15 is used to test the internal reference voltage. (The default internal reference voltage is 1.19V when the chip is shipped)
  - ✓ Comparator. A set of comparator (The CMP+ port and all ADC input ports can be selected as the positive terminal of the comparator. So the comparator can be used as a multi-channel comparator for time division multiplexing)
  - ✓ Touch key: The microcontroller supports up to 16 touch keys. Every touch key can be enabled independently. The internal reference voltage is adjustable with 4 levels. Charge and discharge time settings and internal working frequency settings are flexible. The touch key supports wake-up CPU from low-power mode.
  - ✓ DAC: 8 channels advanced PWM timer can be used as 8 channels DAC
- **GPIO**
  - ✓ Up to 16 GPIOs: P1.0~P1.7(No P1.2), P3.0~P3.7, P5.4
  - ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull outputmode, open drain mode, high-impedance input mode
  - ✓ Except for P3.0 and P3.1, all other I/O ports are in a high-impedance state after power-on. User must set the I/O ports mode before using them. In addition, the internal 4K pull-up resistor of every I/O can be enabled independently.
- **Package**
  - ✓ TSSOP20, QFN20

2. Pinouts



The download steps using ISP and notes are the same as the circumstances in 2.1.2.

3. Pin descriptions

Pin number		name	type	description
TSSOP20	QFN20			
1	18	P1.4	I/O	Standard IO port
		ADC4	I	ADC analog input 4
		PWM3P	I/O	Capture of external signal/Positive of PWM3 pulse output
		MISO	I/O	Master Iutput/Slave Onput of SPI
		SDA	I/O	Serial data line of I2C
		TK4	I	Touch key
2	19	P1.5	I/O	Standard IO port
		ADC5	I	ADC analog input 5
		PWM3N	I/O	Capture of external signal/Negative of PWM3 pulse output
		SCLK	I/O	Serial Clock of SPI
		SCL	I/O	Serial Clock line of I2C
		TK5	I	Touch key
3	20	P1.6	I/O	Standard IO port
		ADC6	I	ADC analog input 6
		RxD_3	I	Input of UART 1
		PWM4P	I/O	Capture of external signal/Positive of PWM4 pulse output
		MCLKO_2	O	Main clock output
		XTALO	O	Connect to external oscillator
		TK6	I	Touch key
4	1	P1.7	I/O	Standard IO port
		ADC7	I	ADC analog input 7
		TxD_3	O	Transmit pin of UART 1
		PWM4N	I/O	Capture of external signal/Negative of PWM4 pulse output
		PWM5_2	I/O	Capture of external signal/Pulse output of PWM5
		XTALI	I	Connect to external oscillator
		TK7	I	Touch key
5	2	P1.3	I/O	Standard IO port
		ADC3	I	ADC analog input 3
		MOSI	I/O	Master Output/Slave Input of SPI
		PWM2N	I/O	Capture of external signal/Negative of PWM2 pulse output
		T2CLKO	O	Clock out of timer 2
		CMPO_2	O	Output of comparator
		TK7	I	Touch key
6	3	TCAP	I	Charge and discharge capacitance of Touch key
7	4	P5.4	I/O	Standard IO port
		NRST	I	Reset pin (low level reset)
		MCLKO	O	Main clock output
		SS	I	Slave selection of SPI (it is output with regard to master)
		PWM2P	I/O	Capture of external signal/Positive of PWM2 pulse output
		PWM6_2	I/O	Capture of external signal/Pulse output of PWM6
		T2	I	Timer2 external input
		ADC2	I	ADC analog input 2
		TK2	I	Touch key
		ADC_ETR	I	ADC external trigger pin
8	5	Vcc	Vcc	Power Supply
		AVcc	Vcc	ADC Power Supply

Pin number		name	type	description
TSSOP20	QFN20			
9	6	ADC_VRef+	I	Reference voltage pin of ADC, which can be directly connected to the VCC of the MCU when the requirements are not high
10	7	Gnd	Gnd	Ground
		AGnd	Gnd	ADC Ground
11	8	P3.0	I/O	Standard IO port
		RxD	I	Input of UART1
		INT4	I	External interrupt4
		ADC8	I	ADC analog input 8
		TK8	I	Touch key
12	9	P3.1	I/O	Standard IO port
		TxD	O	Transmit pin of UART 1
		ADC9	I	ADC analog input 9
		TK9	I	Touch key
13	10	P3.2	I/O	Standard IO port
		INT0	I	External interrupt0
		SCLK_4	I/O	Serial Clock of SPI
		SCL_4	I/O	Serial Clock line of I2C
		PWMETI	I	PWM external trigger input pin
		PWMET2	I	PWM external trigger input pin 2
		ADC10	I	ADC analog input 10
		TK10	I	Touch key
14	11	P3.3	I/O	Standard IO port
		INT1	I	External interrupt1
		MISO_4	I/O	Master Iutput/Slave Onput of SPI
		SDA_4	I/O	Serial data line of I2C
		PWM4N_4	I/O	Capture of external signal/Negative of PWM4 pulse output
		PWM7_2	I/O	Capture of external signal/Pulse output of PWM7
		ADC11	I	ADC analog input 11
		TK11	I	Touch key
15	12	P3.4	I/O	Standard IO port
		T0	I	Timer0 external input
		T1CLKO	O	Clock out of timer 1
		MOSI_4	I/O	Master Output/Slave Input of SPI
		PWM4P_4	I/O	Capture of external signal/Positive of PWM4 pulse output
		PWM8_2	I/O	Capture of external signal/Pulse output of PWM8
		CMPO	O	Output of comparator
		ADC12	I	ADC analog input 12
		TK12	I	Touch key
16	13	P3.5	I/O	Standard IO port
		T1	I	Timer1 external input
		T0CLKO	O	Clock out of timer 0
		SS_4	I	Slave selection of SPI (it is output with regard to master)
		PWMFLT	I	Enhance PWMA external anomaly detection pin
		PWMFLT2	I	Enhance PWMB external anomaly detection pin
		ADC13	I	ADC analog input 13
		TK13	I	Touch key

Pin number		name	type	description
TSSOP20	QFN20			
17	14	P3.6	I/O	Standard IO port
		INT2	I	External interrupt2
		RxD_2	I	Input of UART1
		CMP-	I	Negative input of comparator
		ADC14	I	ADC analog input 14
		TK14	I	Touch key
18	15	P3.7	I/O	Standard IO port
		INT3	I	External interrupt3
		TxD_2	O	Transmit pin of UART 1
		CMP+	I	Positive input of comparator
		TK15	I	Touch key
19	16	P1.0	I/O	Standard IO port
		ADC0	I	ADC analog input 0
		PWM1P	I/O	Capture of external signal/ Positive of PWMA pulse output
		RxD2	I	Input of UART2
		TK0	I	Touch key
		CMP+_2	I	Positive input of comparator
20	17	P1.1	I/O	Standard IO port
		ADC1	I	ADC analog input 1
		PWM1N	I/O	Capture of external signal/ Negative of PWMA pulse output
		TxD2	I	Transmit pin of UART 2
		TK1	I	Touch key
		CMP+_3	I	Positive input of comparator