1 Overview

STC8F family of MCUs are single clock/machine cycle (which is also called 1T) microcontrollers produced by STC Co. Ltd. It is a new generation of 8051 core MCU with wide voltage range, high speed, high reliability, low power and super strong anti- interference. STC8F family of MCUs use STC ninth generation encryption technology so that they can not be decrypted. They have a fully compatible instruction set with traditional 8051 family of microcontroller. With the enhancedkernel, STC8F family of MCUs are faster than the traditional 8051 MCU at about 11.2~13.2 times.

High precision of ±0.3% R/C clock is integrated in MCU with ±1% temperature drift under the temperature range of -40℃ to +85℃, and ±0.6% temperature drift under normal temperature range from -20℃ to +65℃. The frequency of RC clock can be set from 5MHz to 30MHz when programming a MCU using ISP. Moreover, high reliable reset circuit with 4 level optional reset threshold voltage is integrated in MCU. So, external expensive crystal and the external reset circuit can be eliminated completely.

There are three optional clock sources inside the MCU, internal 24MHz high precision IRC, internal 32KHz low speed IRC, external 4MHz~33MHz oscillator or external clock signal. The clock source can be freely chosen in the user code. After the clock source is selected, it can be 8-bit divided freely, and then be supplied to the CPU and the peripherals.

Two low power modes are provided in MCU: the IDLE mode and the STOP mode. In IDLE mode, CPU stops executing instructions, but all peripherals are still working. At this moment, the power consumption is about 1.5mA at 6MHz working frequency. The STOP mode is the power off mode. At this momont, the CPU and all peripherals stop working, and the power consumption can be reduced to about 0.1uA.

Rich digital peripherals and analog peripherals are provided in MCU, including 4 serial ports, 5 timers, 4 sets of PCA, 8 groups of enhanced PWM and I2C, SPI, 16 channels 12 bit ADC and comparator, which can meet almost all the needs of users when designing a product.

The enhanced dual data pointers are integrated in the STC8F family of microcontrollers. Using program control, the function of automatic increasing or decreasing of data pointer and automatic switching of two sets of data pointers can be realized.

Product	UART	Timers	ADC	Enhanced PWM	PCA	Comparator	I^2C	SPI
STC8F8K64S4A10	●	●	●	●	●	●	●	●
STC8A8K64S4A12	●	●	●	●	●	●	●	●
STC8F2K64S4	●	●			●	●	●	●

2 Features

2.1 Features and Prices of STC8A4K64S2A12 family

✓ **Prices of different selections**

Microcontroller Model	Operating Voltage(V)	Flash Program Memory 100K times bytes	Large Capacity Expansion SRAM bytes	Powerful dual DPTR Increase or Decrease	EEPROM 100K times bytes	I/O maximum number	Serial ports Power-down wake-up	SPI	I²C	Timer/Counter(External Pow-down Wake-up)	16 bits advanced PWM Timers	15 bits Enhanced PWM(Dead Zone Control)	PCA/CCP/PWM(can be external interrupt)	Power-down wake-up timer	15 High speed ADC(8 PWM as 8 D/A use)	Comparators(1 A/D、ext brownout detection)	Internal Low-vol Detection interrupt Pow-wk	Watchdog Reset timer	Internal Reset(optional reset threshold vol)	Internal Clock(24MHz Adjustable)	External clock output and reset	Program encrypted transmission	Set password for next update procedure	Support RS485 download	Support USB download	Online simulation	Footprint				
																											LQFP64S	QFN64 <8x8mm>	LQFP48	QFN48 <6x6mm>	LQFP44	PDIP40
STC8A4K16S2A12	2.0-5.5	16K	4K	2	48K	59	2	Yes	Yes	5	-	8	4	Yes	12b	Yes	Yes	Yes	4lev	Yes	Yes	Yes	Yes	Yes	Yes	Yes	¥3.1		¥2.9		¥2.9	
STC8A4K32S2A12	2.0-5.5	32K	4K	2	32K	59	2	Yes	Yes	5	-	8	4	Yes	12b	Yes	Yes	Yes	4lev	Yes	Yes	Yes	Yes	Yes	Yes	Yes	¥3.3		¥3.0		¥3.0	
STC8A4K60S2A12	2.0-5.5	60K	4K	2	4K	59	2	Yes	Yes	5	-	8	4	Yes	12b	Yes	Yes	Yes	4lev	Yes	Yes	Yes	Yes	Yes	Yes	Yes	¥3.6		¥3.2		¥3.2	
STC8A4K64S2A12	2.0-5.5	64K	4K	2	IAP	59	2	Yes	Yes	5	-	8	4	Yes	12b	Yes	Yes	Yes	4lev	Yes	Yes	Yes	Yes	Yes	Yes	Yes	¥3.6		¥3.2		¥3.2	

- ✓ **Core**
  - ✓ Enhanced 8051 Core with single clock per machine cycle (1T)
  - ✓ Fully compatible instruction set with traditional 8051
  - ✓ 20 interrupt sources and 4 interrupt priority levels
  - ✓ Online debugging is supported
- ✓ **Operating voltage**
  - ✓ 2.0 to 5.5V
  - ✓ Built-in LDO
- ✓ **Operating temperature**
  - ✓ -40℃~85℃
- ✓ **Flash memory**
  - ✓ Up to 64Kbytes of Flash memory to be used to store user code
  - ✓ Configurable EEPROM size, 512bytes single page erased, can be repeatedly erased more than 100 thousand times.
  - ✓ In-System-Programming, ISP in short, can be used to update the application code, no need for programmer.

- ✓ Online debugging with single chip is supported, and no emulator is needed. The number of breakpoints is unlimited theoretically.

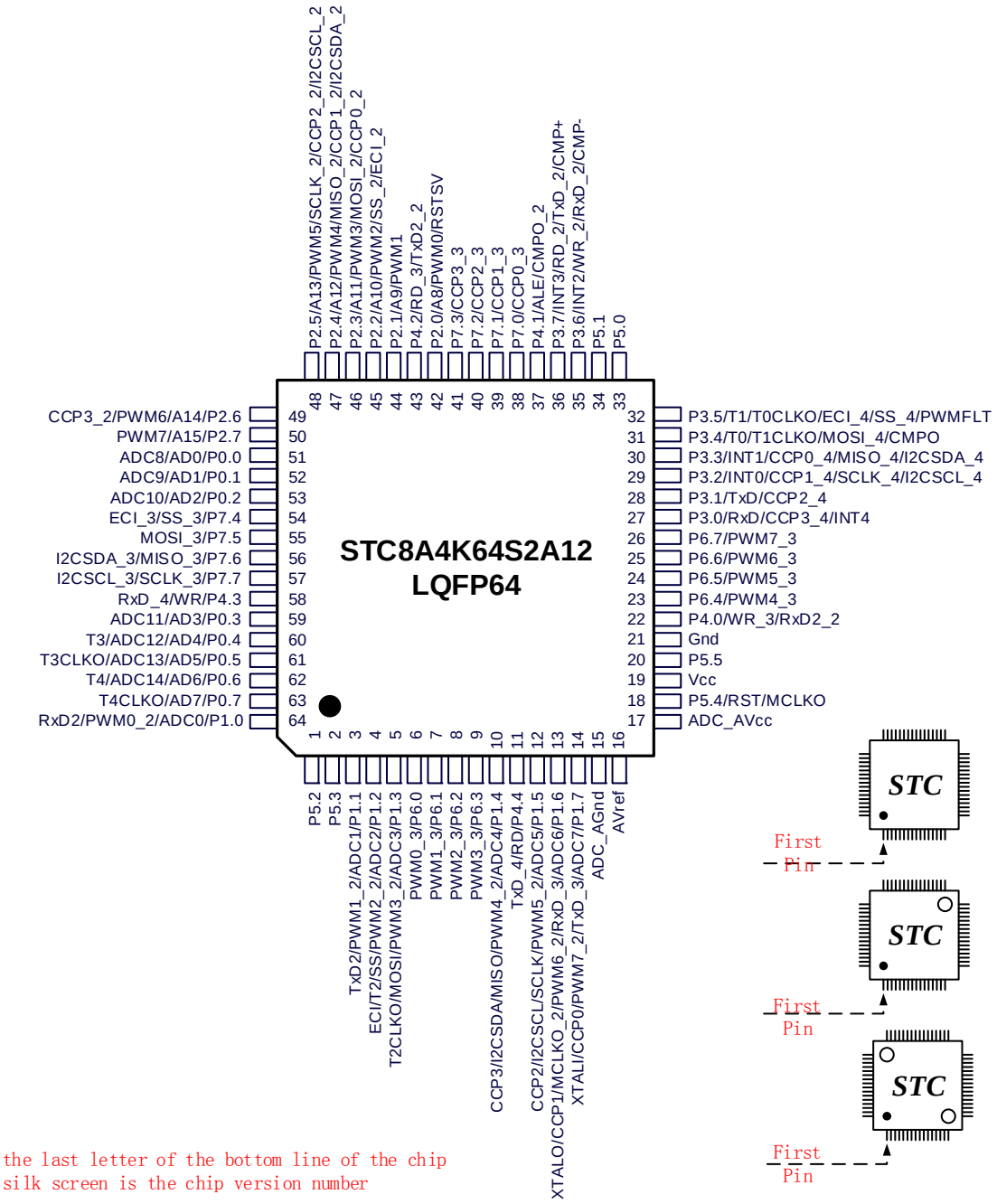
- ✓ **SRAM**
  - ✓ 128 bytes internal direct access RAM
  - ✓ 128 bytes internal indirect access RAM
  - ✓ 4096 bytes internal extended RAM
  - ✓ RAM expandable externally up to 64 Kbytes
- ✓ **Clock**
  - ✓ Internal 24MHz high precise R/C clock IRC
    - ⌖ Error: ±0.3%
    - ⌖ Temperature drift: ±1.0% at the temperature range of -40℃ to 85℃ and ±0.6% at the temperature range of -20℃ to 65℃
  - ✓ Internal 32KHz low speed IRC with large error
  - ✓ External 4MHz~33MHz oscillator or external clock
    The three clock source above can be selected freely by used code.
- ✓ **Reset**
  - ✓ Hardware reset
    - ⌖ Power-on reset
    - ⌖ Reset by reset pin with high reset pulse
    - ⌖ Watch dog timer reset
    - ⌖ Low voltage detection reset. 4 low voltage detection levels are provided, 2.2V, 2.4V, V2.7, V3.0
  - ✓ Software reset
    - ⌖ Writing the reset trigger register using software
- ✓ **Interrupts**
  - ✓ 20 interrupt sources: INT0, INT1, INT2, INT3, INT4, timer0, timer1, timer2, timer3, timer4, uart1, uart2, ADC, LVD, PCA/CCP, SPI, I^2C, comparator, enhanced PWM, enhanced PWM fault detection
  - ✓ 4 interrupt priority levels
- ✓ **Digital peripherals**
  - ✓ 5 16-bit timers: timer0, timer1, timer2, timer3, timer4. Where the mode 3 of timer0 has the Non Maskable Interrupt (NMI in short) function. Mode 0 of timer0 and timer1 is 16-bit Auto-reload mode.
  - ✓ 2 high speed UARTs: uart1, uart2,uart3, uart4, whose baud rate clock source may be fast as FOSC/4
  - ✓ 4 groups of PCA: CCP0, CCP1, CCP2, CCP3, which can be used as capture, high speed output and 6-bits, 7-bits, 8-bits or 10-bits PWM
  - ✓ 8 groups of 15 bit enhanced PWM. Control signal with dead zone can be realized, and external fault detection function is supported.
  - ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
  - ✓ I^2C: Master mode or slave mode are supported.
- ✓ **Analog peripherals**
  - ✓ ADC: 15 channels 12 bit ADC
  - ✓ Comparator

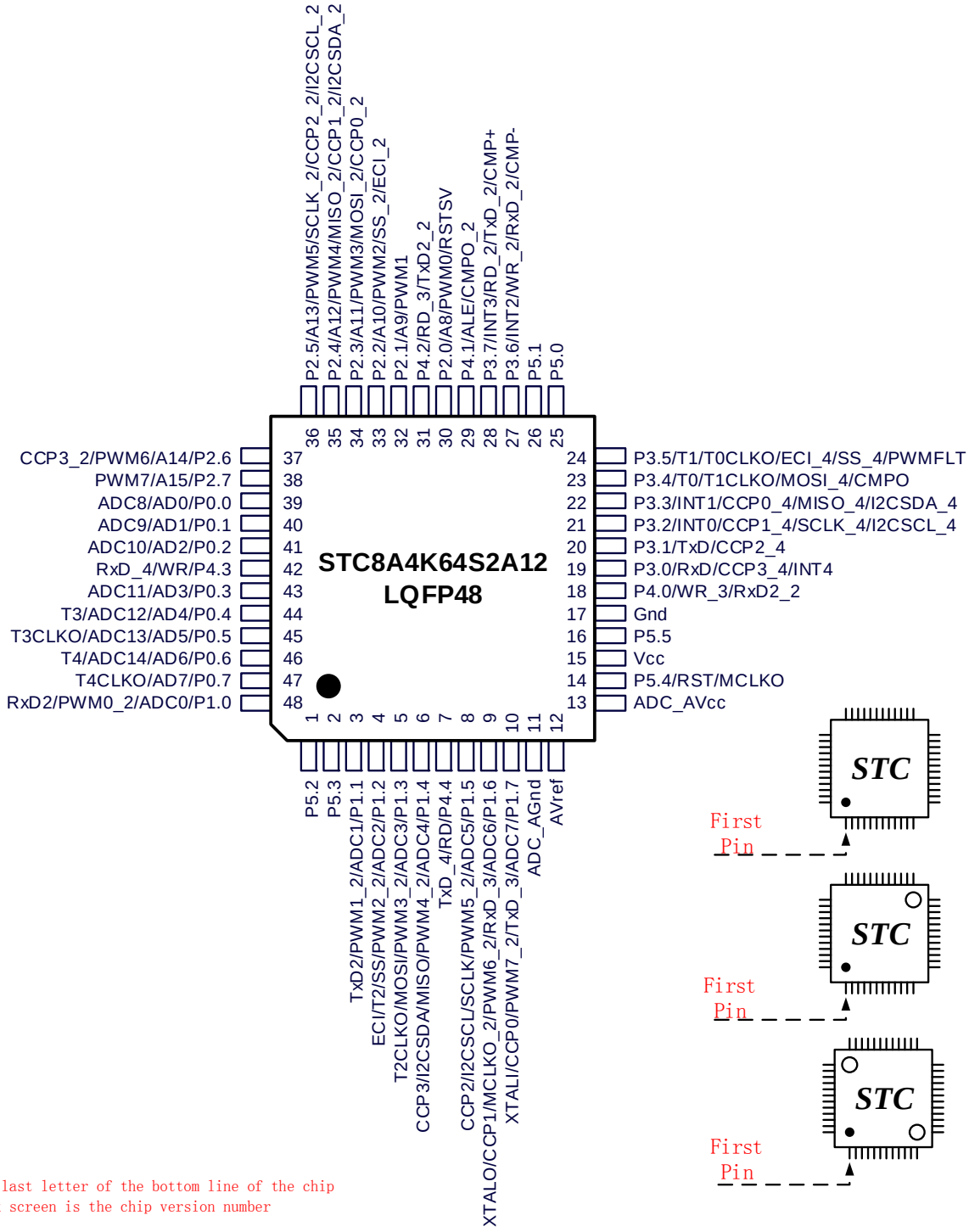
- ✓ **GPIO**
  - ✓ Up to 59 GPIOs: P0.0~P0.7, P1.0~P1.7, P2.0~P2.7, P3.0~P3.7, P4.0~P4.4, P5.0~P5.5, P6.0~P6.7, P7.0~P7.7
  - ✓ 4 modes for all GPIOs: quasi-bidirectional mode, push-pull output mode, open drain mode, high-impedance input mode
- ✓ **Package**
  - ✓ LQFP64, LQFP48, LQFP44

3 Pinouts and pin descriptions

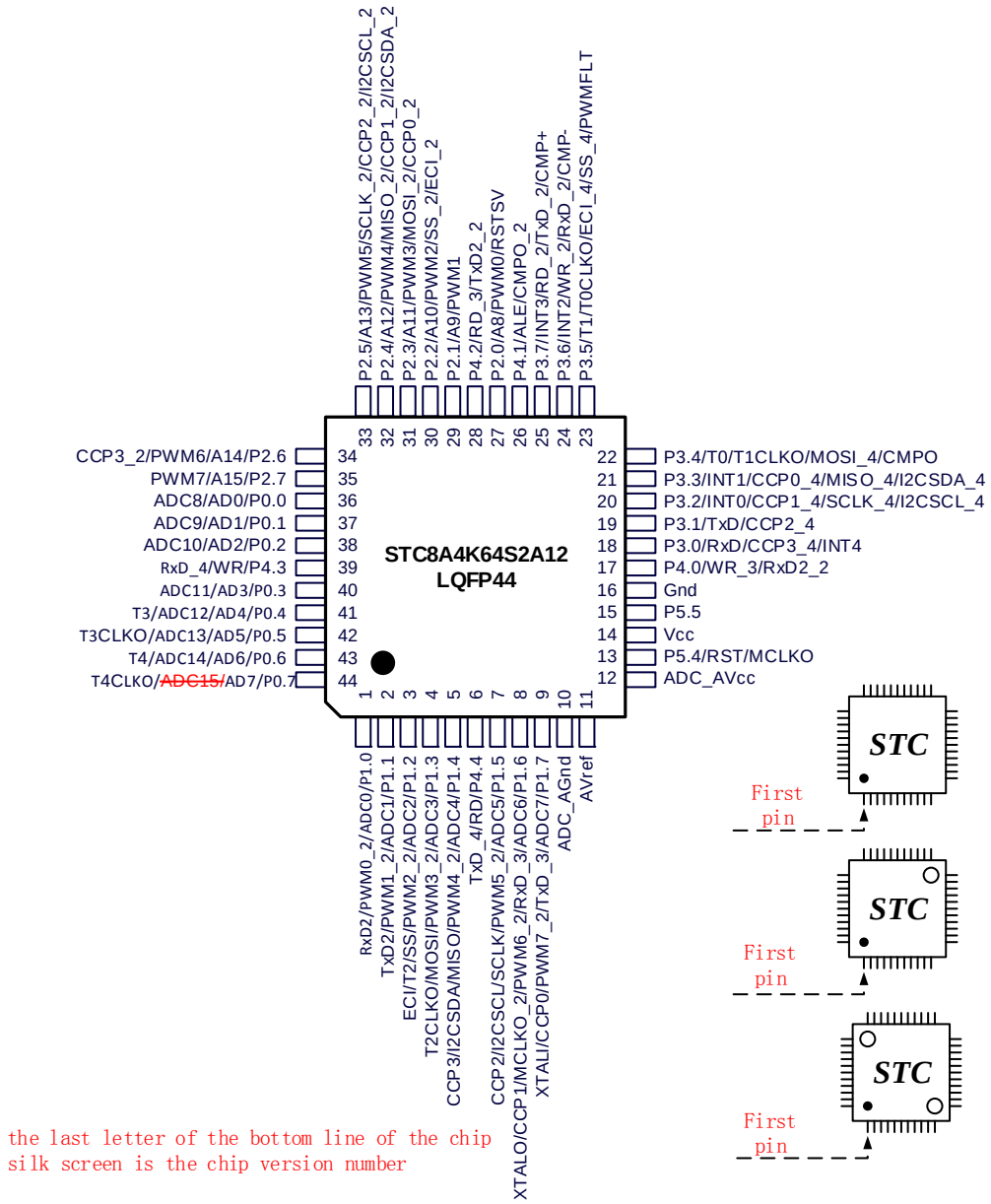
3.1 Pinouts

3.1.1 STC8A4K64S2A12 family pinouts

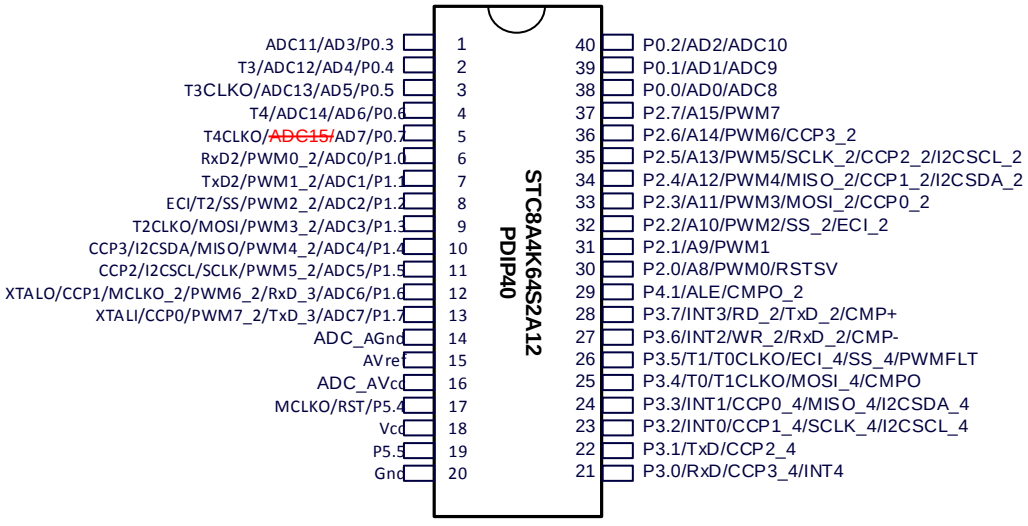




the last letter of the bottom line of the chip silk screen is the chip version number



the last letter of the bottom line of the chip silk screen is the chip version number



3.2 Pin descriptions

3.2.1 STC8A4K64S2A12 family pin descriptions

Number				Name	Class	Instruction
LQFP64S	LQFP48	LQFP44	PDIP40			
1	1			P5.2	I/O	Standard IO Pins
2	2			P5.3	I/O	Standard IO Pins
3	3	2	7	P1.1	I/O	Standard IO Pins
				ADC1	I	ADC analog input channel 1
				PWM1_2	O	Enhanced PWM channel 1 output pin
				TxD2	O	Serial Port 2 Transport Pin
4	4	3	8	P1.2	I/O	Standard IO Pins
				ADC2	I	ADC analog input channel 2
				PWM2_2	O	Enhanced PWM channel 2 output pin
				SS	I/O	SPI Slave selection
				T2	I	Timer 2 external clock input
				ECI	I	PCA external pulse input
5	5	4	9	P1.3	I/O	Standard IO Pins
				ADC3	I	ADC analog input channel 3
				PWM3_2	O	Enhanced PWM channel 3 output pin
				MOSI	I/O	SPI master output slave input
				T2CLKO	O	Timer 2 clock frequency output
6				P6.0	I/O	Standard IO Pins
				PWM0_3	O	Enhanced PWM channel 0 output pin
7				P6.1	I/O	Standard IO Pins
				PWM1_3	O	Enhanced PWM channel 1 output pin
8				P6.2	I/O	Standard IO Pins
				PWM2_3	O	Enhanced PWM channel 2 output pin
9				P6.3	I/O	Standard IO Pins
				PWM3_3	O	Enhanced PWM channel 3 output pin

Number				Name	Class	Instruction
LQFP64S	LQFP48	LQFP44	PDIP40			
10	6	5	10	P1.4	I/O	Standard IO port
				ADC4	I	ADC analog input channel 4
				PWM4_2	O	Enhanced PWM channel 4 output pin
				MISO	I/O	SPI master input slave output
				SDA	I/O	I2C INTERFACE DATA LINE
				CCP3	I/O	PCA capture input and pulse output
11	7	6		P4.4	I/O	Standard IO port
				RD	O	External bus read signal line
				TxD_4	O	Serial Port 1 Transport Pin
12	8	7	11	P1.5	I/O	Standard IO port
				ADC5	I	ADC analog input channel 5
				PWM5_2	O	Enhanced PWM channel 5 output pin
				SCLK	I/O	SPI CLOCK LINE
				SCL	I/O	I2C CLOCK LINE
				CCP2	I/O	PCA capture input and pulse output
13	9	8	12	P1.6	I/O	Standard IO port
				ADC6	I	ADC analog input channel 6
				RxD_3	I	Serial Port 1 Receive Pin
				PWM6_2	O	Enhanced PWM channel 6 output pin
				MCLKO_2	O	Main clock frequency output
				CCP1	I/O	PCA capture input and pulse output
				XTALO	O	Output pin of external crystal
14	10	9	13	P1.7	I/O	Standard IO port
				ADC7	I	ADC analog input channel 7
				TxD_3	O	Serial Port 1 Transport Pin
				PWM7_2	O	Enhanced PWM channel 7 output pin
				CCP0	I/O	PCA capture input and pulse output
				XTALI	I	External crystal/external clock input pin
15	11	10	14	ADC_AGnd	GND	ADC GND
16	12	11	15	AVref	I	ADC reference voltage pin
17	13	12	16	ADC_AVcc	VCC	ADC SOURCE PIN
18	14	13	17	P5.4	I/O	Standard IO port
				RST	I	Reset pin
				MCLKO	O	Main clock frequency output
19	15	14	18	Vcc	VCC	VCC
20	16	15	19	P5.5	I/O	Standard IO port
21	17	16	20	Gnd	GND	GND

Number				Name	Class	Instruction
LQFP64S	LQFP48	LQFP44	PDIP40			
22	18	17		P4.0	I/O	Standard IO port
				WR_3	O	External bus write signal line
				RxD2_2	I	Serial Port 2 Receive Pin
23				P6.4	I/O	Standard IO port
				PWM4_3	O	Enhanced PWM channel 4 output pin
24				P6.5	I/O	Standard IO port
				PWM5_3	O	Enhanced PWM channel 5 output pin
25				P6.6	I/O	Standard IO port
				PWM6_3	O	Enhanced PWM channel 6 output pin
26				P6.7	I/O	Standard IO port
				PWM7_3	O	Enhanced PWM channel 7 output pin
27	19	18	21	P3.0	I/O	Standard IO port
				RxD	I	Serial Port 1 Receive Pin
				CCP3_4	I/O	PCA capture input and pulse output
				INT4	I	External interrupt 4
28	20	19	22	P3.1	I/O	Standard IO port
				TxD	O	Serial Port 1 Transport Pin
				CCP2_4	I/O	PCA capture input and pulse output
29	21	20	23	P3.2	I/O	Standard IO port
				INT0	I	External interrupt 0
				CCP1_4	I/O	PCA capture input and pulse output
				SCLK_4	I/O	SPI CLOCK LINE
				SCL_4	I/O	I2C CLOCK LINE
30	22	21	24	P3.3	I/O	Standard IO port
				INT1	I	External interrupt 1
				CCP0_4	I/O	PCA capture input and pulse output
				MISO_4	I/O	SPI master input slave output
				SDA_4	I/O	I2C INTERFACE DATA LINE
31	23	22	25	P3.4	I/O	Standard IO port
				T0	I	Timer 0 external clock input
				T1CLKO	O	Timer 1 clock frequency output
				MOSI_4	I/O	SPI master output slave input
				CMPO	O	Comparator output

Number				Name	Class	Instruction
LQFP64S	LQFP48	LQFP44	PDIP40			
32	24	23	26	P3.5	I/O	Standard IO port
				T1	I	Timer 1 external clock input
				T0CLKO	O	Timer 0 clock divider output
				ECI_4	I	PCA EXTERNAL PULSE INPUT
				SS_4	I	SPI slave select pin (host output)
				PWMFLT	I	Enhanced PWM external anomaly detection pin
33	25			P5.0	I/O	Standard IO port
34	26			P5.1	I/O	Standard IO port
35	27	24	27	P3.6	I/O	Standard IO port
				INT2	I	External interrupt 2
				WR_2	O	External bus write signal line
				RxD_2	I	Serial Port 1 Receive Pin
				CMP-	I	Comparator negative input
36	28	25	28	P3.7	I/O	Standard IO port
				INT3	I	External interrupt3
				RD_2	O	External bus read signal line
				TxD_2	O	Serial Port 1 Transport Pin
				CMP+	I	Comparator positive input
37	29	26	29	P4.1	I/O	Standard IO port
				ALE	O	Address latch signal
				CMPO_2	O	Comparator output
38				P7.0	I/O	Standard IO port
				CCP0_3	I/O	PCA capture input and pulse output
39				P7.1	I/O	Standard IO port
				CCP1_3	I/O	PCA capture input and pulse output
40				P7.2	I/O	Standard IO port
				CCP2_3	I/O	PCA capture input and pulse output
41				P7.3	I/O	Standard IO port
				CCP3_3	I/O	PCA capture input and pulse output
42	30	27	30	P2.0	I/O	Standard IO port
				A8	I	Address bus
				PWM0	O	Enhanced PWM channel 0 output pin
				RSTSV	-	the port can be configured during ISP download
43	31	28		P4.2	I/O	Standard IO port
				RD_3	O	External bus read signal line
				TxD2_2	O	Serial Port 2 Transport Pin

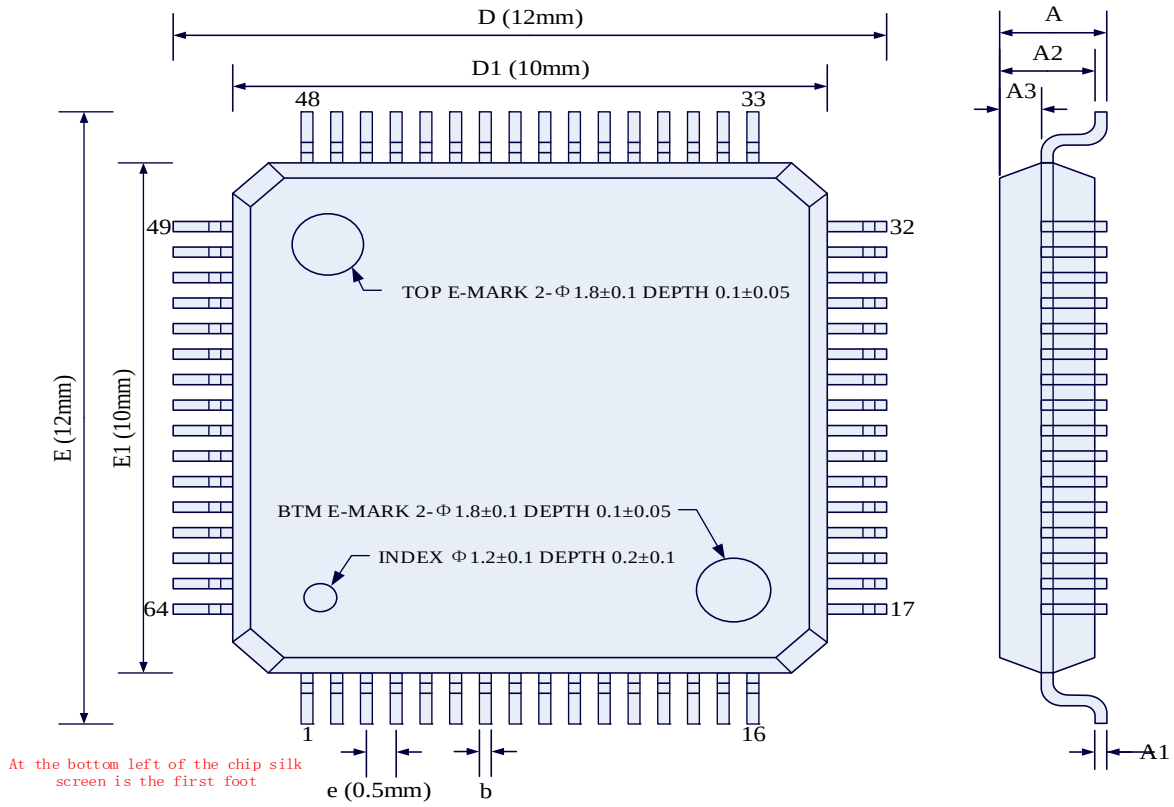
Number				Name	Class	Instruction
LQFP64S	LQFP48	LQFP44	PDIP40			
44	32	29	31	P2.1	I/O	Standard IO port
				A9	I	Address bus
				PWM1	O	Enhanced PWM channel 1 output pin
45	33	30	32	P2.2	I/O	Standard IO port
				A10	I	Address bus
				PWM2	O	Enhanced PWM channel 2 output pin
				SS_2	I	SPI slave select pin (host output)
				ECI_2	I	PCA EXTERNAL PULSE INPUT
46	34	31	33	P2.3	I/O	Standard IO port
				A11	I	Address bus
				PWM3	O	Enhanced PWM channel 3 output pin
				MOSI_2	I/O	SPI master output slave input
				CCP0_2	I/O	PCA capture input and pulse output
47	35	32	34	P2.4	I/O	Standard IO port
				A12	I	Address bus
				PWM4	O	Enhanced PWM channel 4 output pin
				MISO_2	I/O	SPI master input slave output
				SDA_2	I/O	I2C INTERFACE DATA LINE
				CCP1_2	I/O	PCA CAPTURE INPUT AND PULSE OUTPUT
48	36	33	35	P2.5	I/O	Standard IO port
				A13	I	Address bus
				PWM5	O	Enhanced PWM channel 5 output pin
				SCLK_2	I/O	SPI CLOCK LINE
				SCL_2	I/O	I2C CLOCK LINE
				CCP2_2	I/O	PCA capture input and pulse output
49	37	34	36	P2.6	I/O	Standard IO port
				A14	I	Address bus
				PWM6	O	Enhanced PWM channel 6 output pin
				CCP3_2	I/O	PCA capture input and pulse output
50	38	35	37	P2.7	I/O	Standard IO port
				A15	I	Address bus
				PWM7	O	Enhanced PWM channel 7 output pin
51	39	36	38	P0.0	I/O	Standard IO port
				AD0	I	Address bus
				ADC8	I	ADC analog input channel 8

Number				Name	Class	Instruction
LQFP64S	LQFP48	LQFP44	PDIP40			
52	40	37	39	P0.1	I/O	Standard IO port
				AD1	I	Address bus
				ADC9	I	ADC analog input channel 9
53	41	38	40	P0.2	I/O	Standard IO port
				AD2	I	Address bus
				ADC10	I	ADC analog input channel 10
54				P7.4	I/O	Standard IO port
				SS_3	I	SPI slave select pin (host output)
				ECI_3	I	PCA EXTERNAL PULSE INPUT
55				P7.5	I/O	Standard IO port
				MOSI_3	I/O	SPI master output slave input
56				P7.6	I/O	Standard IO port
				MISO_3	I/O	SPI master input slave output
				SDA_3	I/O	I2C INTERFACE DATA LINE
57				P7.7	I/O	Standard IO port
				SCLK_3	I/O	SPI CLOCK LINE
				SCL_3	I/O	I2C CLOCK LINE
58	42	39		P4.3	I/O	Standard IO port
				WR	O	External bus write signal line
				RxD_4	I	Serial Port 1 Receive Pin
59	43	40	1	P0.3	I/O	Standard IO port
				AD3	I	Address bus
				ADC11	I	ADC analog input channel 11
60	44	41	2	P0.4	I/O	Standard IO port
				AD4	I	Address bus
				ADC12	I	ADC analog input channel 12
				T3	I	Timer 3 external clock input

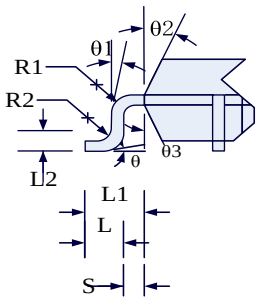
Number				Name	Class	Instruction
LQFP64S	LQFP48	LQFP44	PDIP40			
61	45	42	3	P0.5	I/O	Standard IO port
				AD5	I	Address bus
				ADC13	I	ADC analog input channel 13
				T3CLKO	O	Timer 3 clock frequency output
62	46	43	4	P0.6	I/O	Standard IO port
				AD6	I	Address bus
				ADC14	I	ADC analog input channel 14
				T4	I	Timer 4 external clock input
63	47	44	5	P0.7	I/O	Standard IO port
				AD7	I	Address bus
				T4CLKO	O	Timer 4 clock frequency output
64	48	1	6	P1.0	I/O	Standard IO port
				ADC0	I	ADC analog input channel 0
				PWM0_2	O	Enhanced PWM channel 0 output pin
				RxD2	I	Serial Port 2 Receive Pin

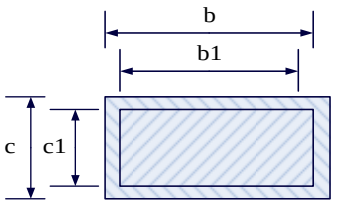
4 Package characteristics

4.1 LQFP64S package mechanical data（12mm*12mm）



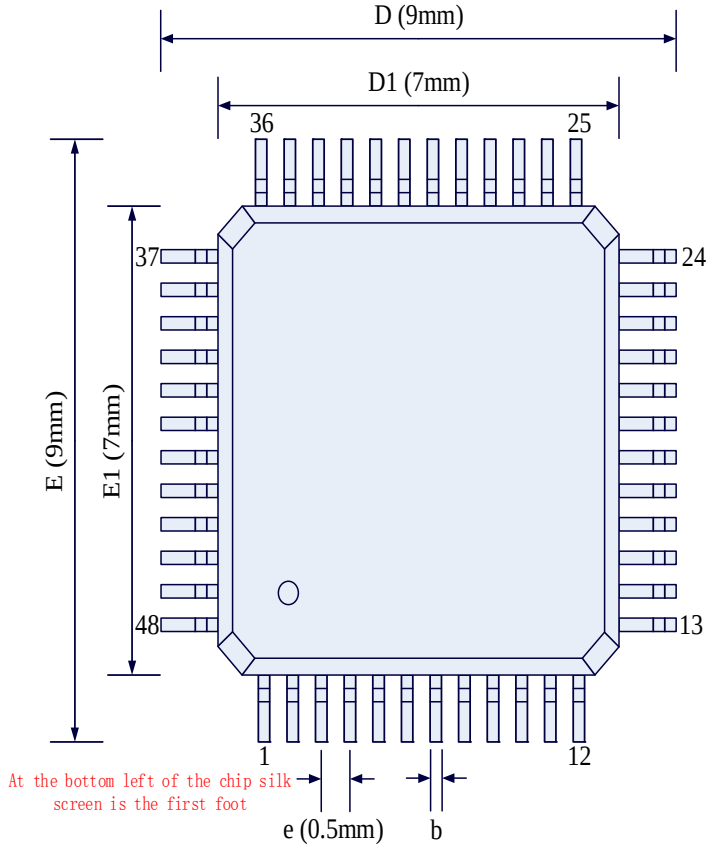
general size			
units of measurement： mm			
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°



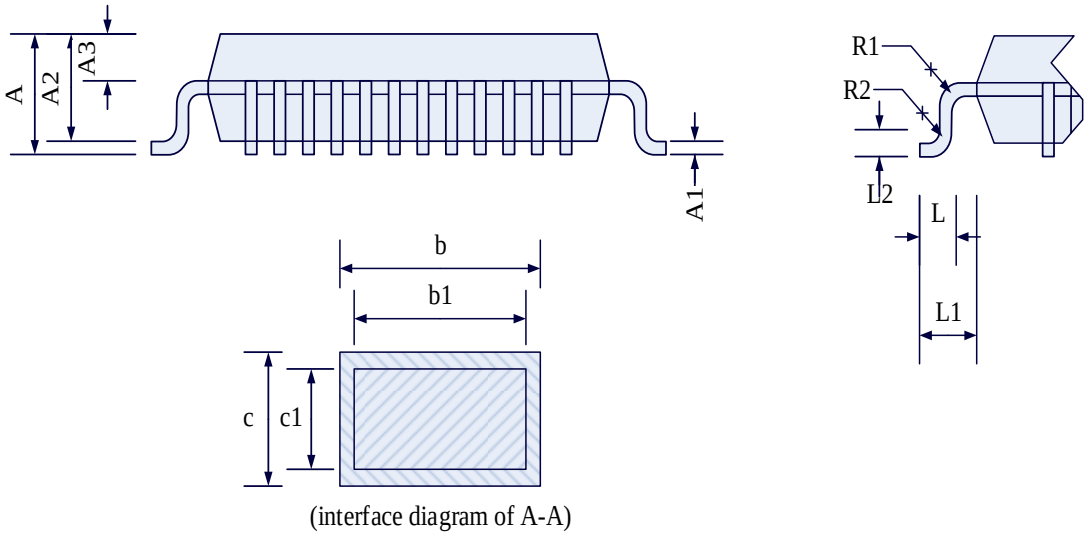


(interface diagram of A-A)

4.2 LQFP48 package mechanical data（9mm*9mm）

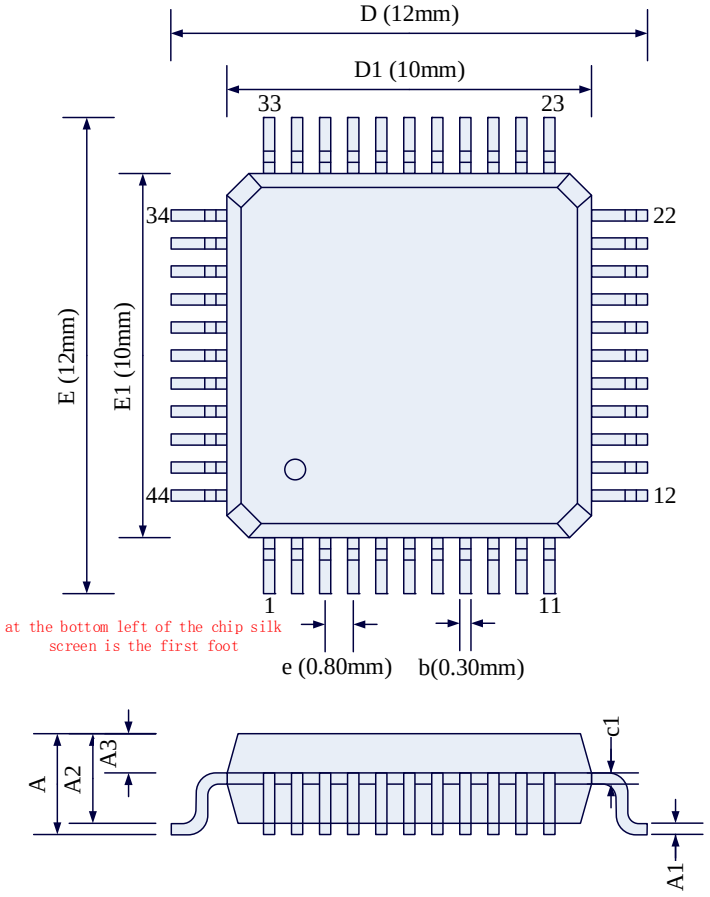


general size			
units of measurement：mm			
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.30	0.35	0.40
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.45	0.50	0.55
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-

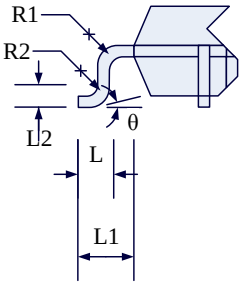


(interface diagram of A-A)

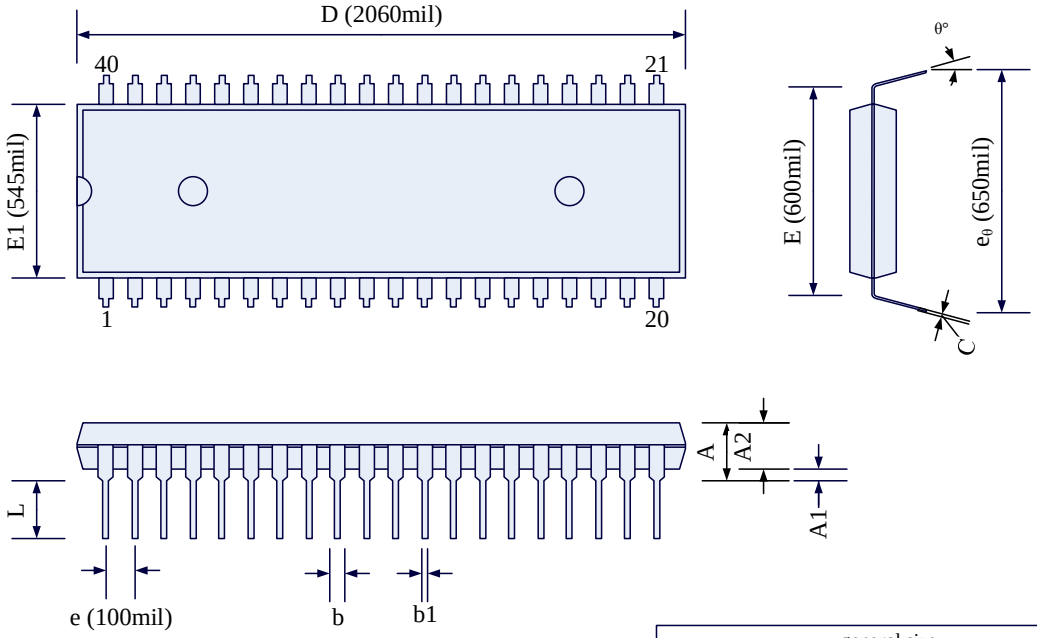
4.3 LQFP44 package mechanical data（12mm*12mm）



general size			
units of measurement：mm			
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.25	0.30	0.35
c1	0.09	-	0.16
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.70	0.80	0.90
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20



4.4 PDIP40 package mechanical data



general size			
units of measurement：mil			
SYMBOL	MIN	TYP	MAX
A	-	-	190
A1	15	-	20
A2	150	155	160
b	45	-	67
b1	15	-	21
C	8	-	15
D	2025	2060	2070
E	600 BSC		
E1	540	545	550
e_θ	630	650	690
L	120	130	140
θ	0°	7°	15°