# STC

## Very Low Power/Voltage CMOS SRAM
## 128K X 16 bit

# STC62WV12816

## ■ FEATURES

- Wide Vcc operation voltage : 2.4V ~ 5.5V
- Very low power consumption :
  - Vcc = 3.0V C-grade: 29mA (@55ns) operating current
    I -grade: 30mA (@55ns) operating current
    C-grade: 24mA (@70ns) operating current
    I -grade: 25mA (@70ns) operating current
    0.3uA(Typ.) CMOS standby current
  - Vcc = 5.0V C-grade: 60mA (@55ns) operating current
    I -grade: 62mA (@55ns) operating current
    C-grade: 53mA (@70ns) operating current
    I -grade: 55mA (@70ns) operating current
    1.0uA(Typ.) CMOS standby current
- High speed access time :
  - -55 55ns
  - -70 70ns
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with $\overline{CE}$ and $\overline{OE}$ options
- I/O Configuration x8/x16 selectable by $\overline{LB}$ and $\overline{UB}$ pin

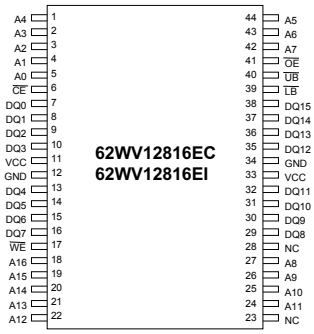
## ■ DESCRIPTION

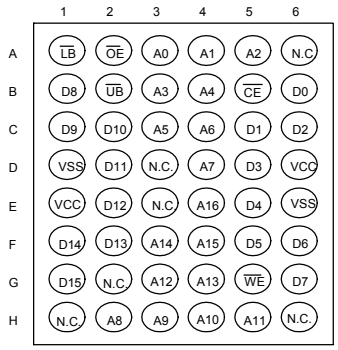
The STC62WV12816 is a high performance , very low power CMOS Static Random Access Memory organized as 131,072 words by 16 bits and operates from a wide range of 2.4V to 5.5V supply voltage.
Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.3uA at 3.0V/25ºC and maximum access time of 55ns at 3.0V/85ºC.
Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$), active LOW output enable($\overline{OE}$) and three-state output drivers.
The STC62WV12816 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.
The STC62WV12816 is available in DICE form , JEDEC standard 44-pin TSOP Type II package and 48-ball BGA package.

## ■ PRODUCT FAMILY

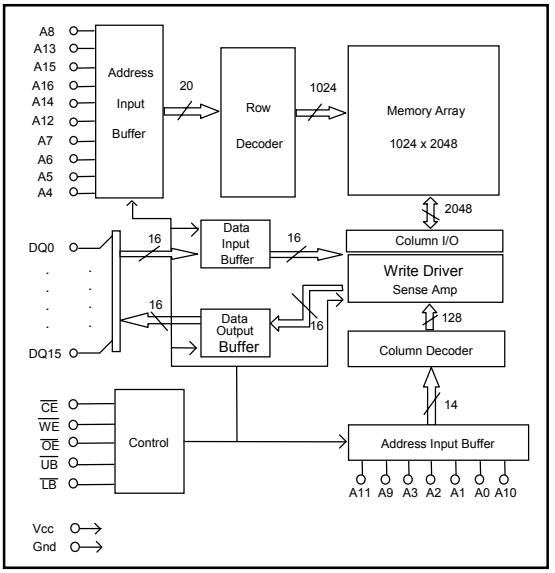
| PRODUCT FAMILY | OPERATING TEMPERATURE | Vcc RANGE | SPEED ( ns ) | POWER DISSIPATION | | | | PKG TYPE |
|---|---|---|---|---|---|---|---|---|
| | | | | STANDBY ( $I_{CCSB1}$, Max ) | | Operating ( $I_{CC}$, Max ) | | |
| | | | 55ns: 3.0~5.5V<br>70ns: 2.7~5.5V | Vcc=3.0V | Vcc=5.0V | Vcc=3.0V<br>70ns | Vcc=5.0V<br>70ns | |
| STC62WV12816DC | +0 ºC to +70 ºC | 2.4V ~5.5V | 55/70 | 3.0uA | 10uA | 24mA | 53mA | DICE |
| STC62WV12816EC | | | | | | | | TSOP2-44 |
| STC62WV12816AC | | | | | | | | BGA-48-0608 |
| STC62WV12816DI | -40 ºC to +85 ºC | 2.4V ~ 5.5V | 55/70 | 5.0uA | 30uA | 25mA | 55mA | DICE |
| STC62WV12816EI | | | | | | | | TSOP2-44 |
| STC62WV12816AI | | | | | | | | BGA-48-0608 |

## ■ PIN CONFIGURATIONS




## ■ BLOCK DIAGRAM



## ■ PIN DESCRIPTIONS

| Name | Function |
|---|---|
| **A0-A16 Address Input** | These 17 address inputs select one of the 131,072 x 16-bit words in the RAM. |
| **$\overline{CE}$ Chip Enable Input** | $\overline{CE}$ is active LOW. Chip enables must be active when data read from or write to the device. if chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected. |
| **$\overline{WE}$ Write Enable Input** | The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location. |
| **$\overline{OE}$ Output Enable Input** | The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive. |
| **$\overline{LB}$ and $\overline{UB}$ Data Byte Control Input** | Lower byte and upper byte data input/output control pins. |
| **DQ0 - DQ15 Data Input/Output Ports** | These 16 bi-directional ports are used to read data from or write data into the RAM. |
| **Vcc** | Power Supply |
| **Gnd** | Ground |

## ■ TRUTH TABLE

| MODE | $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{LB}$ | $\overline{UB}$ | D0~D7 | D8~D15 | Vcc CURRENT |
|---|---|---|---|---|---|---|---|---|
| Not selected (Power Down) | H | X | X | X | X | High Z | High Z | $I_{CCSB}$ , $I_{CCSB1}$ |
| | X | X | X | H | H | High Z | High Z | $I_{CCSB}$ , $I_{CCSB1}$ |
| Output Disabled | L | X | X | H | H | High Z | High Z | $I_{CC}$ |
| | L | H | H | X | X | High Z | High Z | $I_{CC}$ |
| Read | L | H | L | L | L | Dout | Dout | $I_{CC}$ |
| | | | | H | L | High Z | Dout | $I_{CC}$ |
| | | | | L | H | Dout | High Z | $I_{CC}$ |
| Write | L | L | X | L | L | Din | Din | $I_{CC}$ |
| | | | | H | L | X | Din | $I_{CC}$ |
| | | | | L | H | Din | X | $I_{CC}$ |

## ■ ABSOLUTE MAXIMUM RATINGS(1)

| SYMBOL | PARAMETER | RATING | UNITS |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to Vcc+0.5 | V |
| $T_{BIAS}$ | Temperature Under Bias | -40 to +85 | °C |
| $T_{STG}$ | Storage Temperature | -60 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 20 | mA |

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ■ OPERATING RANGE

| RANGE | AMBIENT TEMPERATURE | Vcc |
|---|---|---|
| Commercial | 0°C to +70°C | 2.4V ~ 5.5V |
| Industrial | -40°C to +85°C | 2.4V ~ 5.5V |

## ■ CAPACITANCE (1) (TA = 25°C, f = 1.0 MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|---|---|---|---|---|
| CIN | Input Capacitance | VIN=0V | 6 | pF |
| CDQ | Input/Output Capacitance | VI/O=0V | 8 | pF |

1. This parameter is guaranteed and not 100% tested.

## ■ DC ELECTRICAL CHARACTERISTICS ( TA = -40 to + 85°C )

| PARAMETER NAME | PARAMETER | TEST CONDITIONS | | | MIN. | TYP. (1) | MAX. | UNITS |
|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Guaranteed Input Low Voltage(3) | | Vcc =3.0V | | -0.5 | -- | 0.8 | V |
| | | | Vcc =5.0V | | | | | |
| $V_{IH}$ | Guaranteed Input High Voltage(3) | | Vcc =3.0V | | 2.0 | -- | $V_{cc}$+0.3 | V |
| | | | Vcc =5.0V | | 2.2 | | | |
| $I_{IL}$ | Input Leakage Current | Vcc = Max, $V_{IN}$ = 0V to Vcc | | | -- | -- | 1 | uA |
| $I_{LO}$ | Output Leakage Current | Vcc = Max, $\overline{CE}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$, $V_{I/O}$ = 0V to Vcc | | | -- | -- | 1 | uA |
| $V_{OL}$ | Output Low Voltage | Vcc = Max, $I_{OL}$ = 2.0mA | Vcc =3.0V | | -- | -- | 0.4 | V |
| | | | Vcc =5.0V | | | | | |
| $V_{OH}$ | Output High Voltage | Vcc = Min, $I_{OH}$ = -1.0mA | Vcc =3.0V | | 2.4 | -- | -- | V |
| | | | Vcc =5.0V | | | | | |
| $I_{CC}$(5) | Operating Power Supply Current | $\overline{CE}$ = $V_{IL}$, $I_{DQ}$ = 0mA, F = Fmax(2) | Vcc =3V | 70ns | -- | -- | 25 | mA |
| | | | Vcc =5V | 70ns | | | 55 | |
| $I_{CCSB}$ | Standby Current-TTL | $\overline{CE}$=$V_{IH}$ $I_{DQ}$ = 0mA | Vcc =3.0V | | -- | -- | 0.5 | mA |
| | | | Vcc =5.0V | | | | 1.0 | |
| $I_{CCSB1}$(4) | Standby Current-CMOS | $\overline{CE}$ ≧ Vcc-0.2V, $V_{IN}$ ≧ Vcc-0.2V or $V_{IN}$ ≦ 0.2V | Vcc =3.0V | | -- | 0.3 | 5 | uA |
| | | | Vcc =5.0V | | | 1.0 | 30 | |

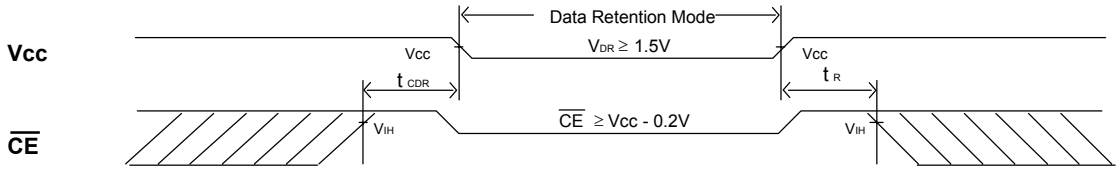
**1**. Typical characteristics are at $T_A$ = 25°C. **2**. Fmax = $1/t_{RC}$.
**3**. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
**4**.$I_{CCSB1_Max.}$ is 3uA/10uA at Vcc=3V/5V and $T_A$=70°C. **5**. $I_{CC_Max.}$ is 30mA(@3V)/62mA(@5V) under 55ns operation.

## ■ DATA RETENTION CHARACTERISTICS ( TA = -40 to + 85°C )

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN. | TYP. (1) | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{DR}$ | Vcc for Data Retention | $\overline{CE}$ ≧ Vcc - 0.2V $V_{IN}$ ≧ Vcc - 0.2V or $V_{IN}$ ≦ 0.2V | 1.5 | -- | -- | V |
| $I_{CCDR}$ (3) | Data Retention Current | $\overline{CE}$ ≧ Vcc - 0.2V $V_{IN}$ ≧ Vcc - 0.2V or $V_{IN}$ ≦ 0.2V | -- | 0.1 | 1.0 | uA |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | See Retention Waveform | 0 | -- | -- | ns |
| $t_R$ | Operation Recovery Time | | $T_{RC}$ (2) | -- | -- | ns |

**1**. Vcc = 1.5V, $T_A$ = + 25°C **2**. $t_{RC}$ = Read Cycle Time **3**. $I_{CCDR_MAX.}$ is 0.7uA at $T_A$=70°C.

## ■ LOW $V_{CC}$ DATA RETENTION WAVEFORM ( $\overline{CE}$ Controlled )




## ■AC TEST CONDITIONS

**(Test Load and Input/Output Reference)**

| | |
|---|---|
| Input Pulse Levels | Vcc / 0V |
| Input Rise and Fall Times | 1V/ns |
| Input and Output Timing Reference Level | 0.5Vcc |
| Output Load | $C_L$ = 100pF+1TTL<br>$C_L$ = 30pF+1TTL |

## ■ KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | MUST BE STEADY | MUST BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGE FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGE FROM L TO H |
| | DON'T CARE: ANY CHANGE PERMITTED | CHANGE : STATE UNKNOWN |
| | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE "OFF "STATE |

## ■ AC ELECTRICAL CHARACTERISTICS ( TA = -40 to + 85°C )

**READ CYCLE**

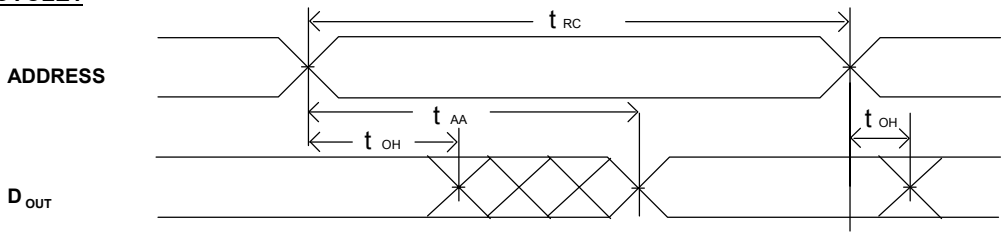
| JEDEC PARAMETER NAME | PARAMETER NAME | DESCRIPTION | | CYCLE TIME : 55ns (Vcc = 3.0~5.5V) MIN. | TYP. | MAX. | CYCLE TIME : 70ns (Vcc = 2.7~5.5V) MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{AVAX}$ | $t_{RC}$ | Read Cycle Time | | 55 | -- | -- | 70 | -- | -- | ns |
| $t_{AVQV}$ | $t_{AA}$ | Address Access Time | | -- | -- | 55 | -- | -- | 70 | ns |
| $t_{ELQV}$ | $t_{ACS}$ | Chip Select Access Time | ($\overline{CE}$) | -- | -- | 55 | -- | -- | 70 | ns |
| $t_{BA}$ | $t_{BA}$ (1) | Data Byte Control Access Time | ($\overline{LB}$,$\overline{UB}$) | -- | -- | 30 | -- | -- | 35 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Valid | | -- | -- | 30 | -- | -- | 35 | ns |
| $t_{E1LQX}$ | $t_{CLZ}$ | Chip Select to Output Low Z | ($\overline{CE}$) | 10 | -- | -- | 10 | -- | -- | ns |
| $t_{BE}$ | $t_{BE}$ | Data Byte Control to Output Low Z | ($\overline{LB}$,$\overline{UB}$) | 10 | -- | -- | 10 | -- | -- | ns |
| $t_{GLQX}$ | $t_{OLZ}$ | Output Enable to Output in Low Z | | 5 | -- | -- | 5 | -- | -- | ns |
| $t_{EHQZ}$ | $t_{CHZ}$ | Chip Deselect to Output in High Z | ($\overline{CE}$) | -- | -- | 30 | -- | -- | 35 | ns |
| $t_{BDO}$ | $t_{BDO}$ | Data Byte Control to Output High Z | ($\overline{LB}$,$\overline{UB}$) | -- | -- | 30 | -- | -- | 35 | ns |
| $t_{GHQZ}$ | $t_{OHZ}$ | Output Disable to Output in High Z | | -- | -- | 25 | -- | -- | 30 | ns |
| $t_{AXOX}$ | $t_{OH}$ | Data Hold from Address Change | | 10 | -- | -- | 10 | -- | -- | ns |

NOTE :

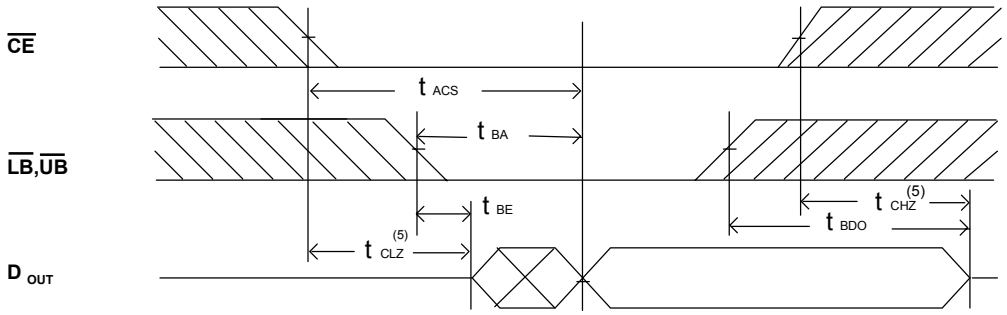
1. $t_{BA}$ is 30ns/35ns (@speed=55ns/70ns) with address toggle. ; $t_{BA}$ is 55ns/70ns (@speed=55ns/70ns) without address toggle.

## ■ SWITCHING WAVEFORMS (READ CYCLE)

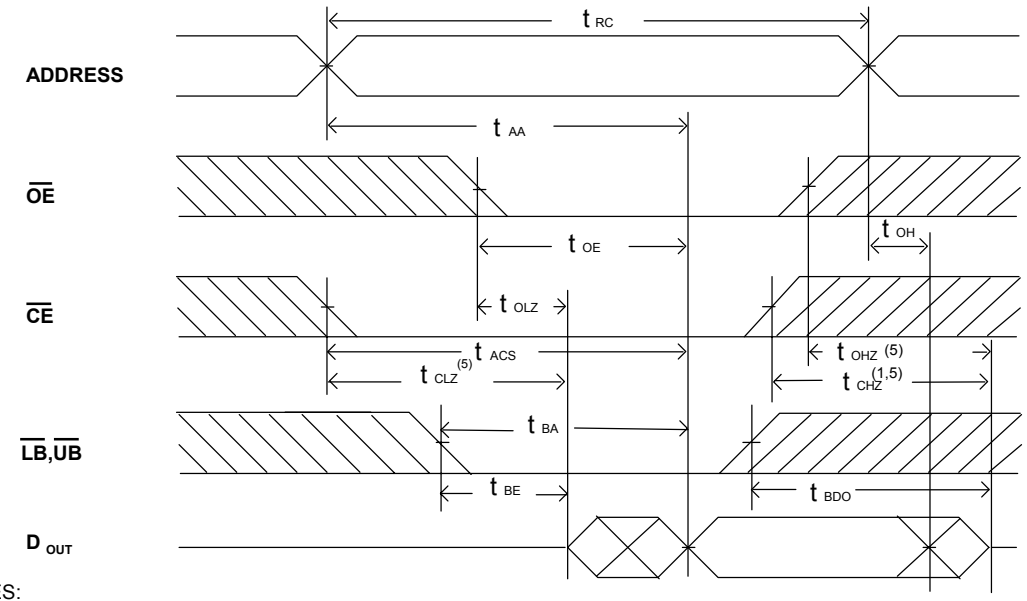
**READ CYCLE1** (1,2,4)




**READ CYCLE2** (1,3,4)




**READ CYCLE3** (1,4)




NOTES:
1. $\overline{WE}$ is high for read Cycle.
2. Device is continuously selected when $\overline{CE}$ = $V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = $V_{IL}$ .
5. The parameter is guaranteed but not 100% tested.

## ■ AC ELECTRICAL CHARACTERISTICS ( TA = -40 to + 85ºC )

### WRITE CYCLE

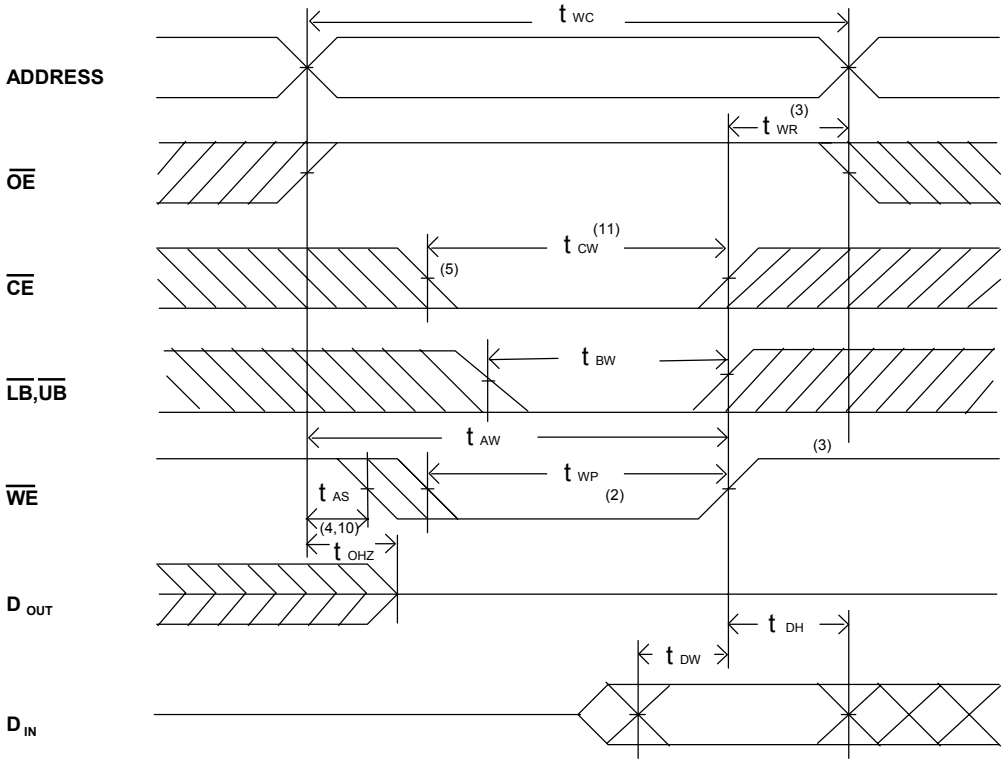
| JEDEC PARAMETER NAME | PARAMETER NAME | DESCRIPTION | CYCLE TIME : 55ns (Vcc = 3.0~5.5V) MIN. | TYP. | MAX. | CYCLE TIME : 70ns (Vcc = 2.7~5.5V) MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{AVAX}$ | $t_{WC}$ | Write Cycle Time | 55 | -- | -- | 70 | -- | -- | ns |
| $t_{E1LWH}$ | $t_{CW}$ | Chip Select to End of Write ($\overline{CE}$) | 55 | -- | -- | 70 | -- | -- | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | 0 | -- | -- | 0 | -- | -- | ns |
| $t_{AVWH}$ | $t_{AW}$ | Address Valid to End of Write | 55 | -- | -- | 70 | -- | -- | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | 30 | -- | -- | 35 | -- | -- | ns |
| $t_{WHAX}$ | $t_{WR}$ | Write recovery Time ($\overline{CE}$,$\overline{WE}$) | 0 | -- | -- | 0 | -- | -- | ns |
| $t_{BW}$ | $t_{BW}$ (1) | Date Byte Control to End of Write ($\overline{LB}$,$\overline{UB}$) | 25 | -- | -- | 30 | -- | -- | ns |
| $t_{WLQZ}$ | $t_{WHZ}$ | Write to Output in High Z | -- | -- | 25 | -- | -- | 30 | ns |
| $t_{DVWH}$ | $t_{DW}$ | Data to Write Time Overlap | 25 | -- | -- | 30 | -- | -- | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold from Write Time | 0 | -- | -- | 0 | -- | -- | ns |
| $t_{GHQZ}$ | $t_{OHZ}$ | Output Disable to Output in High Z | -- | -- | 25 | -- | -- | 30 | ns |
| $t_{WHOX}$ | $t_{OW}$ | End of Write to Output Active | 5 | -- | -- | 5 | -- | -- | ns |

NOTE :

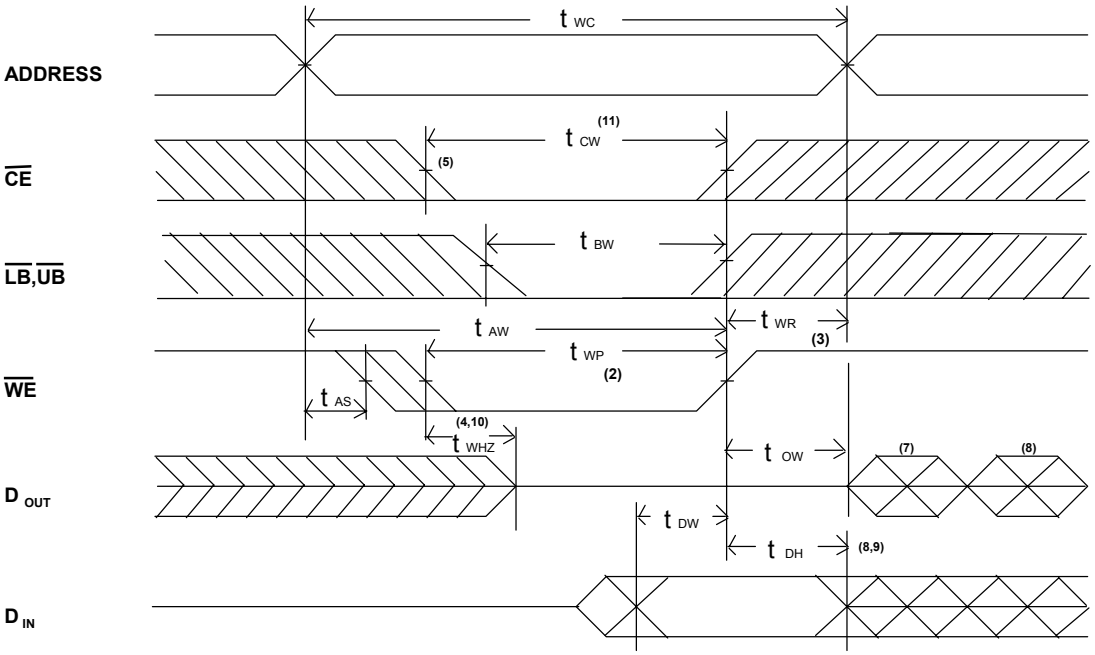
1. $t_{BW}$ is 25ns/30ns (@speed=55ns/70ns) with address toggle. ; $t_{BW}$ is 55ns/70ns (@speed=55ns/70ns) without address toggle.

## ■ SWITCHING WAVEFORMS (WRITE CYCLE)

### WRITE CYCLE1 (1)



**WRITE CYCLE2** (1,6)




NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. $T_{WR}$ is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = $V_{IL}$ ).
7. $D_{OUT}$ is the same phase of write data of this write cycle.
8. $D_{OUT}$ is the read data of next address.
9. If $\overline{CE}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. The parameter is guaranteed but not 100% tested.
11. $T_{CW}$ is measured from the later of $\overline{CE}$ going low to the end of write.

## ■ ORDERING INFORMATION

**STC62WV12816** X X Z Y Y

**SPEED**
55: 55ns
70: 70ns

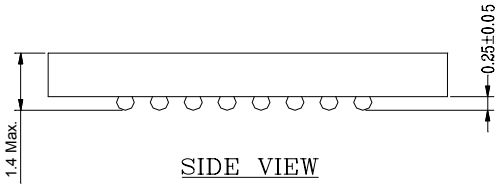
**PKG MATERIAL**
-: Normal
G: Green
P: Pb free

**GRADE**
C: +0°C ~ +70°C
I: -40°C ~ +85°C

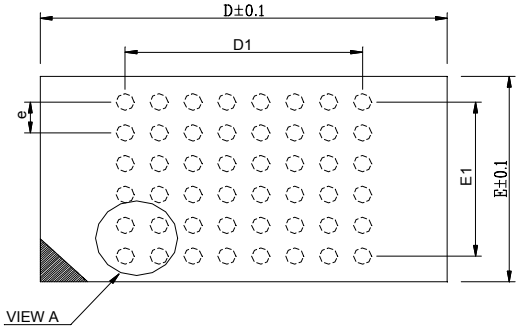
**PACKAGE**
E: TSOP2-44
A: BGA-48-0608
D: DICE

Note:
STC (STC International Limited.) assumes no responsibility for the application or use of any product or circuit described herein. STC does not authorize its products for use as critical components in any application in which the failure of the STC product may be expected to result in significant injury or death, including life-support systems and critical medical instruments.

## ■ PACKAGE DIMENSIONS



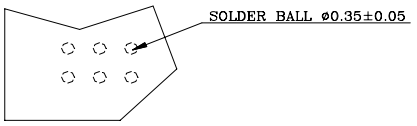

SIDE VIEW




TOP VIEW

NOTES:
1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

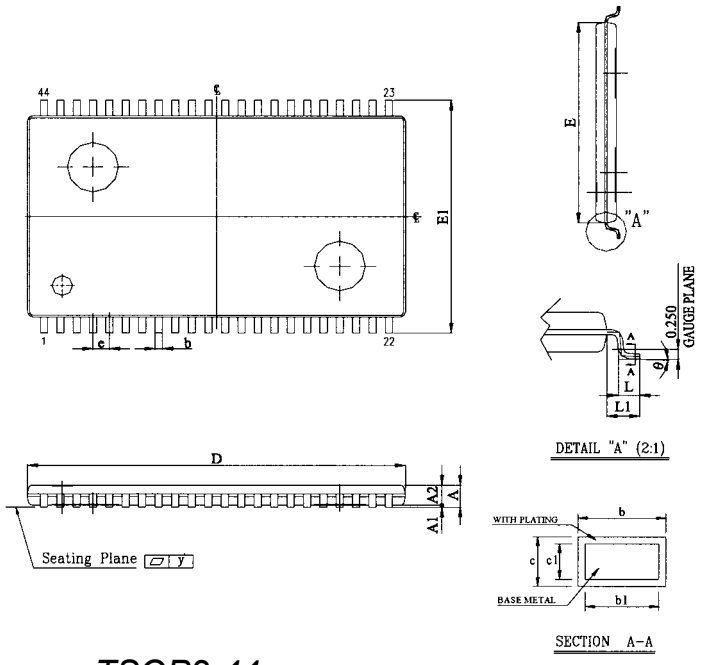
| BALL PITCH e = 0.75 | | | | |
|---|---|---|---|---|
| D | E | N | D1 | E1 |
| 8.0 | 6.0 | 48 | 5.25 | 3.75 |




VIEW A

*48 mini-BGA (6 x 8)*

## ■ PACKAGE DIMENSIONS




| SYMBOL \ UNIT | INCH | MM |
|---|---|---|
| A | 0.0433± 0.004 | 1.10± 0.10 |
| A1 | 0.004± 0.002 | 0.10± 0.05 |
| A2 | 0.039± 0.002 | 1.00± 0.05 |
| b | 0.012 ~ 0.018 | 0.30 ~ 0.45 |
| b1 | 0.012 ~ 0.016 | 0.30 ~ 0.40 |
| c | 0.005 ~ 0.008 | 0.12 ~ 0.21 |
| c1 | 0.005 ~ 0.006 | 0.12 ~ 0.16 |
| D | 0.725± 0.004 | 18.41± 0.10 |
| E | 0.400± 0.004 | 10.16± 0.10 |
| E1 | 0.463± 0.008 | 11.76± 0.20 |
| e | 0.0315± 0.004 | 0.80± 0.10 |
| L | 0.0197± 0.004 | 0.50± 0.10 |
| L1 | 0.0315± 0.004 | 0.80± 0.10 |
| y | 0.004 Max. | 0.1 Max. |
| θ | 0° ~ 8° | 0° ~ 8° |

*TSOP2-44*