

STC32CL8K64-33A-TSSOP20, Package Under Verification

1. Features and Price

Selection Guide (No external crystal / external reset required, 12-bit ADC, 10 channels)

products supply information				
Price & Package		TSSOP20 <6.5mm*6.5mm>		
Online debug itself			Y	Y
Support RS485 download			Y	Y
Password can be set for next update			Y	Y
Program encrypted transmission (Anti-blocking)			Y	Y
Clock output and Reset			Y	Y
Internal high precision Clock (adjustable under 42MHz)			Y	Y
Internal high reliable reset circuit with 4 levels optional reset threshold voltage			Y	Y
Watch-dog Timer			Y	Y
Internal LVD interrupt (can wake-up CPU)			Y	Y
Comparator (May be used as ADC to detect external power-down)			Y	Y
DMA 15 channels high speed ADC (8 PWMs can be used as 8 DACs)			12bit	12bit
Power-down Wake-up timer			Y	Y
16-bit advanced PWM timer with Complementary symmetrical dead-time			8	8
Timers/Counters (T0-T4 Pin Can wake-up CPU)			5	5
MDU32 (Hardware 32-bit Multiplier and Divider)			Y	Y
DMA I ² C which can wake-up CPU			Y	Y
I2S			Y	Y
DMA SPI which can wake-up CPU			Y	Y
LIN BUS			1	1
CAN BUS			2	2
DMA UARTs which can wake-up CPU			2	2
RTC			Y	Y
All I/O ports support interrupts and can wake up MCU			Y	Y
Traditional I/O interrupt (INT0/INT1/INT2/INT3/INT4) (can wake-up CPU)			Y	Y
Maximum I/O Lines			17	17
EEPROM 100 thousand times (Byte)			16K	16K
xdata Internal extended SRAM (Byte)			6K	6K
Edats/data Internal DATA RAM(Byte)			2K	2K
Flash Code Memory (100 thousand times) (Byte)			48K	64K
Operating voltage (V)			1.9-5.5	1.9-5.5
MCU			STC32CL8K48	STC32CL8K64

➤ Core

- ✓ Ultra-high-speed 32-bit 8051 core (1T), over 70 times faster than traditional 8051 at the same frequency
- ✓ 48 interrupt sources, 4 interrupt priority levels
- ✓ Supports online simulation

➤ Operating Voltage

- ✓ 1.9 V ~ 5.5 V (≥ 3.0 V when operating temperature $< -40^{\circ}\text{C}$)

➤ Operating Temperature

- ✓ $-20^{\circ}\text{C} \sim 65^{\circ}\text{C}$ (Commercial Grade): Internal high-speed IRC drift $-0.76\% \sim +0.98\%$, operating frequency ≤ 42 MHz
- ✓ $-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$ (Industrial Grade): Internal high-speed IRC drift $\pm 1.3\%$, operating frequency ≤ 42 MHz
- ✓ $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$ (AEC-Q100 Grade1): Internal high-speed IRC drift $\pm 3\%$, operating frequency ≤ 33 MHz; external crystal ≤ 24 MHz recommended above 85°C (automotive crystal: ¥0.38)

➤ Flash Memory

- ✓ Up to 64 KB Flash program memory (ROM) for user code
- ✓ User-configurable EEPROM size, 512-byte page erase, $\geq 100,000$ erase/write cycles
- ✓ Supports hardware USB direct download and standard UART download
- ✓ Supports hardware SWD real-time simulation (P3.0/P3.1, requires STC-USB-Link1D)

➤ **SRAM (Total 6 KB)**

- ✓ 2 KB internal SRAM (edata)
- ✓ 6 KB internal extended RAM (xdata)
- ✓ Note: Strongly recommend not using idata and pdata for variable declaration

➤ **Clock Control**

- ✓ Internal high-precision, high-stability high-speed IRC (≤ 42 MHz, selectable or manual input in ISP programming)
 - Error $\pm 0.3\%$ (at 25°C ambient)
 - Drift $-0.76\% \sim +0.98\%$ (Commercial Grade: $-20^{\circ}\text{C} \sim 65^{\circ}\text{C}$, centered at 25°C)
 - Drift $-1.35\% \sim +1.30\%$ (Industrial Grade: $-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$, centered at 25°C)
 - Drift $-3\% \sim +3\%$ (AEC-Q00 Grade1: $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$, centered at 42.5°C)

【Notes】 :

STC32CL8K64-33A running at Automotive Grade 1 temperature range: operating frequency ≤ 33 MHz; typical automotive frequencies: 24/16/12 MHz

Automotive-grade MCU can be used as industrial-grade; operating frequency ≤ 42 MHz in industrial temperature range

Use internal high-speed IRC if no strict requirement for clock accuracy

Use external automotive crystal (¥0.38) for strict clock accuracy requirements

- ✓ Internal 32 kHz low-speed IRC (large error, no temperature/voltage compensation for low power)
- ✓ External crystal (≤ 42 MHz) and external clock
- ✓ Internal PLL output clock (96 MHz / 144 MHz can be used independently for high-speed PWM and high-speed SPI clock source)

Four clock sources are user-selectable

(Power-up sequence: After power-on reset / reset pin reset / watchdog reset / low-voltage detect reset, the chip boots from ISP ROM with fixed 24 MHz high-speed IRC. After user program download and reset, it uses user-configured high-speed IRC. To use external crystal, external 32.768 kHz crystal or internal 32 kHz low-speed IRC, software must enable the corresponding clock and switch via CLKSEL register.)

➤ **Reset**

- ✓ Hardware Reset
 - Power-on reset: 1.7 V $\sim$ 1.9 V (valid when LVD is disabled)
 - Reset pin reset: P5.4 defaults to I/O; can be configured as reset pin in ISP (active low)
 - Watchdog overflow reset
 - Low-voltage detect (LVD) reset: 4 selectable thresholds: 2.0 V, 2.4 V, 2.7 V, 3.0 V
- ✓ Software Reset

Trigger reset by writing to the reset trigger register

➤ **Interrupt**

- ✓ 38 interrupt sources: INT0–INT4, T0–T4, USART1–2, UART3–4, ADC, LVD, SPI, I2C, Comparator, PWMA/B, CAN/CAN2, LIN, RTC, 4 groups of I/O interrupts, DMA UART1–4 TX/RX, DMA I2C TX/RX, DMA SPI, DMA ADC, memory-to-memory DMA interrupt
- ✓ 4 interrupt priority levels

➤ **Digital Peripherals**

- ✓ $5 \times$ 16-bit timers (T0–T4); T0 Mode3 supports NMI (non-maskable interrupt); T0/T1 Mode0: 16-bit auto-reload
 - ✓ $2 \times$ high-speed USART (USART1–2): supports sync/async, SPI, LIN, IrDA, ISO7816; baud rate up to
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FOSC/4

- ✓ 2 × high-speed UART (UART3–4): baud rate up to FOSC/4
- ✓ 2 × advanced PWM: 8 channels (4 complementary pairs) with dead-time control and external fault detection
- ✓ SPI: Master / Slave / auto-switch
- ✓ I2C: Master / Slave
- ✓ ICE: hardware simulation support
- ✓ RTC: year/month/day/hour/minute/second/1/128 second, clock interrupt and one alarm
- ✓ I2S: audio bus
- ✓ CAN: 2 independent CAN 2.0 controllers
- ✓ LIN: 1 independent LIN controller (supports 1.3 and 2.1); USART1 and USART2 support 2 additional LIN channels
- ✓ MDU32: hardware 32-bit multiplier/divider (32-bit × 32-bit, 32-bit ÷ 32-bit)
- ✓ I/O interrupt: all I/O support interrupt; 4 trigger modes (high/low level, rising/falling edge); power-down wakeup, 4 priority levels
- ✓ DMA: SPI TX/RX, I2C TX/RX, UART1–4 TX/RX, ADC auto-sampling to memory (with averaging), LCD driver output, memory-to-memory copy
- ✓ Hardware digital ID: 32 bytes

➤ **Analog Peripherals**

- ✓ ADC: ultra-high speed, 12-bit 15-channel (CH0–CH14); CH15 for internal 1.19 V reference (±1% error)
- ✓ Comparator: 1 channel

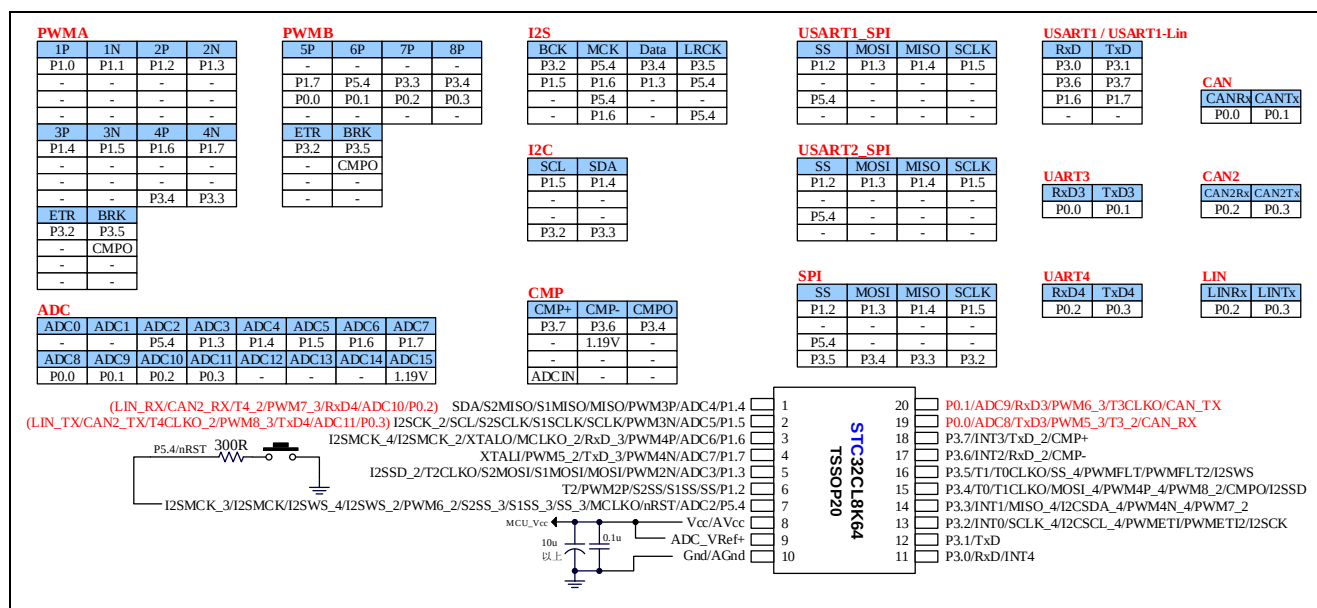
➤ **GPIO**

- ✓ Up to 19 GPIOs: P0.0–P0.3, P1.2–P1.7, P3.0–P3.7, P5.4
- ✓ 4 I/O modes: quasi-bidirectional, push-pull output, open-drain, high-impedance input
- ✓ All I/O except P3.0 and P3.1: high-impedance input at power-up; I/O mode must be set before use
- ✓ Each I/O can independently enable internal 10K pull-up and 10K pull-down resistors

➤ **Package**

- ✓ TSSOP20
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2. Pin Diagram (TSSOP20)



3. ESD and Latch-Up Description for STC32CL8K64-33A

ESD-HBM: above 8000 V

Latch-Up

➤ **Room temperature: Latch-Up current of all I/O ≥ 200 mA (including P2.4 / P3.5)**

➤ **Test Condition: AEC-Q100 Grade 1 (+125°C)**

- ✓ Max operating voltage 3.63 V, $1.5\times$ voltage = 5.445 V:
+800 mA PASS, -800 mA PASS → Level A
 - ✓ Max operating voltage 4.7 V, $1.5\times$ voltage = 7.05 V:
+125 mA PASS, -175 mA PASS → Level A
 - ✓ Max operating voltage 4.8 V, $1.5\times$ voltage = 7.2 V:
+100 mA PASS, -175 mA PASS → Level A
 - ✓ Max operating voltage 4.9 V, $1.5\times$ voltage = 7.35 V:
+75 mA PASS, -175 mA PASS → Level B
 - ✓ Max operating voltage 5.0 V, $1.5\times$ voltage = 7.5 V:
+75 mA PASS, -175 mA PASS → Level B
 - ✓ Max operating voltage 5.1 V, $1.5\times$ voltage = 7.65 V:
+75 mA PASS, -175 mA PASS → Level B
 - ✓ Max operating voltage 5.2 V, $1.5\times$ voltage = 7.8 V:
+75 mA PASS, -175 mA PASS → Level B
 - ✓ Max operating voltage 5.3 V, $1.5\times$ voltage = 7.95 V:
+75 mA PASS, -175 mA PASS → Level B
 - ✓ Max operating voltage 5.4 V, $1.5\times$ voltage = 8.1 V:
+75 mA PASS, -175 mA PASS → Level B
 - ✓ Max operating voltage 5.5 V, $1.5\times$ voltage = 8.25 V, I/O with 200 Ω resistor:
+200 mA PASS, -200 mA PASS → Level A
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➤ **Test Condition: AEC-Q100 Grade 2 (+105°C)**

- ✓ Max operating voltage 5.5 V, 1.5× voltage = 8.25 V:
+100 mA PASS, −175 mA PASS → Level A

Automotive Qualification Sample Description

Sample Name	Automotive-Grade General-Purpose 32-bit MCU
Model Specification	STC32G8K64-33A
Sample Description	STC32G8K64-33A belongs to the STC32G series products of STCAI Company. This series is an automotive-grade general-purpose 32-bit MCU, including 2 sets of CAN, 3 sets of LIN, DMA supporting 4 sets of serial ports, SPI/I2C/ADC, etc., with PWM output, comparator and LVD/LVR reset functions, and up to 45 I/O ports.
	This series has a variety of packages and models to choose from, including LQFP48, LQFP44, LQFP32, QFN48, QFN32, TSSOP20, as follows:
	LQFP48: STC32G8K64-33A, STC32G8K48-33A;
	LQFP44: STC32G8K64-33A, STC32G8K48-33A;
	LQFP32: STC32G8K64-33A, STC32G8K48-33A;
	QFN48: STC32G8K64-33A, STC32G8K48-33A;
	QFN32: STC32G8K64-33A, STC32G8K48-33A;
	TSSOP20: STC32CL8K64-33A, STC32CL8K48-33A

4. Pin Function Description for Different Package Types

TSSOP20	Name	Type	Description
1	P1.4	I/O	Standard I/O port
	ADC4	I	ADC analog input channel 4
	PWM3P	I/O	PWM3 capture input and pulse output positive
	MISO	I/O	SPI Master Input Slave Output
	S1MISO	I/O	USART1 - SPI Master Input Slave Output
	S2MISO	I/O	USART2 - SPI Master Input Slave Output
	SDA	I/O	I2C interface data line
2	P1.5	I/O	Standard I/O port
	ADC5	I	ADC analog input channel 5
	PWM3N	I/O	PWM3 pulse output negative
	SCLK	I/O	SPI clock pin
	S1SCLK	I/O	USART1 - SPI clock pin
	S2SCLK	I/O	USART2 - SPI clock pin
	SCL	I/O	I2C clock line
	I2SBCK_2	I/O	I2S clock line
3	P1.6	I/O	Standard I/O port
	ADC6	I	ADC analog input channel 6
	RxD_3	I	Serial port 1 receive pin
	PWM4P	I/O	PWM4 capture input and pulse output positive
	MCLKO_2	O	Main clock divided output
	XTALO	O	External crystal oscillator output pin
	I2SMCK_2	O	I2S master clock line
	I2SMCK_4	O	I2S master clock line
4	P1.7	I/O	Standard I/O port
	ADC7	I	ADC analog input channel 7
	TxD_3	O	Serial port 1 transmit pin
	PWM4N	I/O	PWM4 pulse output negative
	PWM5_2	I/O	PWM5 capture input and pulse output
	XTALI	I	External crystal / external clock input pin
5	P1.3	I/O	Standard I/O port
	ADC3	I	ADC analog input channel 3
	MOSI	I/O	SPI Master Output Slave Input
	S1MOSI	I/O	USART1 - SPI Master Output Slave Input
	S2MOSI	I/O	USART2 - SPI Master Output Slave Input
	PWM2N	I/O	PWM2 pulse output negative
	T2CLKO	O	Timer 2 clock divided output
	I2SData_2	I/O	I2S data line

TSSOP20	Name	Type	Description
6	P1.2	I/O	Standard I/O port
	PWM2P	I/O	PWM2 capture input and pulse output positive
	SS	I	SPI slave select pin (output when master)
	S1SS	I	USART1 - SPI slave select pin (output when master)
	S2SS	I	USART2 - SPI slave select pin (output when master)
	T2	I	Timer 2 external clock input
	ADC_ETR	I	ADC external trigger pin
7	P5.4	I/O	Standard I/O port
	ADC2	I	ADC analog input channel 2
	nRST	I	Reset pin
	MCLKO	O	Main clock divided output
	SS_3	I	SPI slave select pin (output when master)
	S1SS_3	I	USART1 - SPI slave select pin (output when master)
	S2SS_3	I	USART2 - SPI slave select pin (output when master)
	PWM6_2	I/O	PWM6 capture input and pulse output
	I2SLRCK_2	I/O	I2S channel select line
	I2SLRCK_4	I/O	I2S channel select line
	I2SMCK	O	I2S master clock line
	I2SMCK_3	O	I2S master clock line
8	Vcc	VCC	Power supply pin
	AVcc	VCC	ADC power supply pin
9	ADC_VRef+	I	ADC reference voltage pin
10	Gnd	GND	Ground
	Agnd	GND	ADC ground
	VRef-	I	ADC reference voltage ground
11	P3.0	I/O	Standard I/O port
	RxD	I	Serial port 1 receive pin
	INT4	I	External interrupt 4
12	P3.1	I/O	Standard I/O port
	TxD	O	Serial port 1 transmit pin
13	P3.2	I/O	Standard I/O port
	INT0	I	External interrupt 0
	SCLK_4	I/O	SPI clock pin
	SCL_4	I/O	I2C clock line
	PWMETI	I	PWM external trigger input pin
	PWMETI2	I	PWM external trigger input pin 2
	I2SBCK	I/O	I2S clock line

TSSOP20	Name	Type	Description
14	P3.3	I/O	Standard I/O port
	INT1	I	External interrupt 1
	MISO_4	I/O	SPI Master Input Slave Output
	SDA_4	I/O	I2C interface data line
	PWM4N_4	I/O	PWM4 pulse output negative
	PWM7_2	I/O	PWM7 capture input and pulse output
15	P3.4	I/O	Standard I/O port
	T0	I	Timer 0 external clock input
	T1CLKO	O	Timer 1 clock divided output
	MOSI_4	I/O	SPI Master Output Slave Input
	PWM4P_4	I/O	PWM4 capture input and pulse output positive
	PWM8_2	I/O	PWM8 capture input and pulse output
	CMPO	O	Comparator output
	I2SData	I/O	I2S data line
16	P3.5	I/O	Standard I/O port
	T1	I	Timer 1 external clock input
	T0CLKO	O	Timer 0 clock divided output
	SS_4	I	SPI slave select pin (output when master)
	PWMFLT	I	Enhanced PWM external fault detection pin
	I2SLRCK	I/O	I2S channel select line
17	P3.6	I/O	Standard I/O port
	INT2	I	External interrupt 2
	RxD_2	I	Serial port 1 receive pin
	CMP-	I	Comparator negative input
18	P3.7	I/O	Standard I/O port
	INT3	I	External interrupt 3
	TxD_2	O	Serial port 1 transmit pin
	CMP+	I	Comparator positive input
19	P0.0	I/O	Standard I/O port
	ADC8	I	ADC analog input channel 8
	RxD3	I	Serial port 3 receive pin
	PWM5_3	I/O	PWM5 capture input and pulse output
	T3_2	I	Timer 3 external clock input
	CAN_RX	I	CAN bus receive pin
20	P0.1	I/O	Standard I/O port
	ADC9	I	ADC analog input channel 9
	TxD3	O	Serial port 3 transmit pin
	PWM6_3	I/O	PWM6 capture input and pulse output
	T3CLKO_2	O	Timer 3 clock divided output
	CAN_TX	O	CAN bus transmit pin

TSSOP20	Name	Type	Description
1	P0.2	I/O	Standard I/O port
	ADC10	I	ADC analog input channel 10
	RxD4	I	Serial port 4 receive pin
	PWM7_3	I/O	PWM7 capture input and pulse output
	T4_2	I	Timer 4 external clock input
	CAN2_RX	I	CAN2 bus receive pin
	LIN_RX	I	LIN bus receive pin
2	P0.3	I/O	Standard I/O port
	ADC11	I	ADC analog input channel 11
	TxD4	O	Serial port 4 transmit pin
	PWM8_3	I/O	PWM8 capture input and pulse output
	T4CLKO_2	O	Timer 4 clock divided output
	CAN2_TX	O	CAN2 bus transmit pin
	LIN_TX	O	LIN bus transmit pin