General Overview of STC15W4K32S4 series

1. Introduction of STC15W4K32S4 series MCU

STC15W4K32S4 series MCU is a single-chip microcontroller based on a high performance 1T architecture 8051 CPU, which is produced by STC MCU Limited. It is a new generation of 8051 MCU with high speed, high stability, wide voltage range, low power consumption and super strong anti-disturbance. With the enhanced kernel, STC15W4K32S4 series MCU is faster than the traditional 8051 one in executing instructions (about 8~12 times the rate of the traditional 8051 MCU), and has a fully compatible instruction set with traditional 8051 series microcontroller. External expensive crystal can be removed by being integrated internal high-precise R/C clock(±0.3%) with ±1% temperature drift (-40 ~+85) while ±0.6% in normal temperature (-20 ~+65). External reset curcuit also can be removed by being integrated internal highly reliable one with 16 levels optional threshold voltage of reset. The STC15W4K32S4 series MCU retains all features of the traditional 8051 one. In addition, it has 8-channels and 10-bits PWM, 8-channels and 10-bits A/D Converter(300 thousand times per sec.), Comparator, large capacity of 4K bytes SRAM, four high-speed asynchronous serial ports----UARTs(UART1/UART2/UART3/UART4) and a high-speed synchronous serial peripheral interface----SPI.

In Keil C development environment, please choose the Intel 8052 to compiling and only contain < reg51.h > as header file.

STC15 family with super high-speed CPU core of STC-Y5 works 20% faster than STC early 1T series (such as STC12/STC11/STC10 series) in same clock frequency.

- Enhanced 8051 Central Processing Unit, 1T, single clock per machine cycle, faster 8~12 times than the rate of a traditional 8051.
- Operating voltage range : 5.5V ~ 2.5V.
- On-chip 16K/32K/40K/48K/56K/58K/61K/63.5K FLASH program memory with flexible ISP/IAP capability, can be repeatedly erased more than 100 thousand times.
- Large capacity of on-chip 4096 bytes SRAM: 256 byte scratch-pad RAM and 3840 bytes of auxiliary RAM
- Be capable of addressing up to 64K byte of external RAM
- On-chip EEPROM with large capacity can be repeatedly erased more than 100 thousand times.
- Dual Data Pointer (DPTR) to speed up data movement
- ISP/IAP, In-System-Programming and In-Application-Programming , no need for programmer and emulator.
- 8 channels and 10 bits Analog-to-Digital Converter (ADC), the speed up to 300 thousand times per second, 3 channels PWM also can be used as 3 channels D/A Converter(DAC).
- 6 channels 15 bits high-precision PWM (with a dead-section controller) and 2 channels CCP (The high-speed pulse function of which can be utilized to realize 11 ~ 16 bits PWM)
  ---- can be used as 8 channels D/A Converter or 2 Times or 2 external Interrupts (which can be generated on rising or falling edge).
- Internal hghly reliable Reset with 16 levels optional threshold voltage of reset, so that external reset curcuit can be completely removed.

General Overview of STC15W4K32S4 series MCU

- Internal high- precise R/C clock(±0.3%) with ±1% temperature drift (-40 ~+85) while ±0.6% (-20 ~+65) in normal temperature and wide frenquency adjustable between 5MHz and 35MHz (5.5296MHz / 11.0592MHz / 22.1184MHz / 33.1776MHz).
- Operating frequency range: 5- 35MHz, is equivalent to traditional 8051:60~420MHz.
- Four high-speed asynchronous serial ports----UARTs (UART1/UART2/UART3/UART4 can be used simultaneously and regarded as 9 serial ports by shifting among 9 groups of pins):
  UART1(RxD/P3.0, TxD/P3.1) can be switched to (RxD_2/P3.6, TxD_2/P3.7),
  also can be switched to (RxD_3/P1.6, TxD_3/P1.7);
  UART2(RxD2/P1.0, TxD2/P1.1) can be switched to (RxD2_2/P4.6, TxD2_2/P4.7);
  UART3(RxD3/P0.0, TxD3/P0.1) can be switched to (RxD3_2/P5.0, TxD3_2/P5.1)
  UART4(RxD4/P0.2, TxD4/P0.3) can be switched to (RxD4_2/P5.2, TxD4_2/P5.3)
- A high-speed synchronous serial peripheral interface----SPI.
- Support the function of Encryption Download (to protect your code from being intercepted).
- Support the function of RS485 Control
- Code protection for flash memory access, excellent noise immunity, very low power consumption
- Power management mode: Slow-Down mode, Idle mode(all interrupt can wake up Idle mode), Stop/Power-Down mode.
- Timers which can wake up stop/power-down mode: have internal low-power special wake-up Timer.
- Resource which can wake up stop/power-down mode are: INT0/P3.2, INT1/P3.3 (INT0/INT1, may be generated on both rising and falling edges), $\overline{\text{INT2}}$/P3.6, $\overline{\text{INT3}}$/P3.7, $\overline{\text{INT4}}$/P3.0 ($\overline{\text{INT2}}$/$\overline{\text{INT3}}$/$\overline{\text{INT4}}$, only be generated on falling edge); pins CCP0/CCP1; pins RxD/RxD2/RxD3/RxD4; pins T0/T1/T2/T3/T4(their falling edge can wake up if T0/T1/T2/T3/T4 have been enabled before power-down mode, but no interrupts can be generatetd); internal low-power special wake-up Timer.
- 7 Timers/Counters: five 16-bit reloadable Timers/Counters (T0/T1/T2/T3/T4, T0 and T1 are compatible with Timer0/Timer1 of traditional 8051) and 2 Timers which maybe realized by 2 channels CCP. T0/T1/T2/T3/T4 all can independently achieve external programmable clock output (5 channels) .
- Programmable clock output function(output by dividing the frequency of the internal system clock or the input clock of external pin):
  The Programmable clock output of T0 is on P3.5/T0CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T0/P3.4)
  The Programmable clock output of T1 is on P3.4/T1CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T1/P3.5)
  The Programmable clock output of T2 is on P3.0/T2CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T2/P3.1)
  The Programmable clock output of T3 is on P0.4/T3CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T3/P0.5)

The Programmable clock output of T4 is on P0.6/T4CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T4/P0.7)

Five timers/counters in above all can be output by dividing the frequency from 1 to 65536.

The Programmable clock output of master clock is on P5.4/MCLKO, and its frequency can be divided into MCLK/1, MCLK/2, MCLK/4, MCLK/16.

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.

MCLK is the frequency of master clock. MCLKO is the output of master clock.

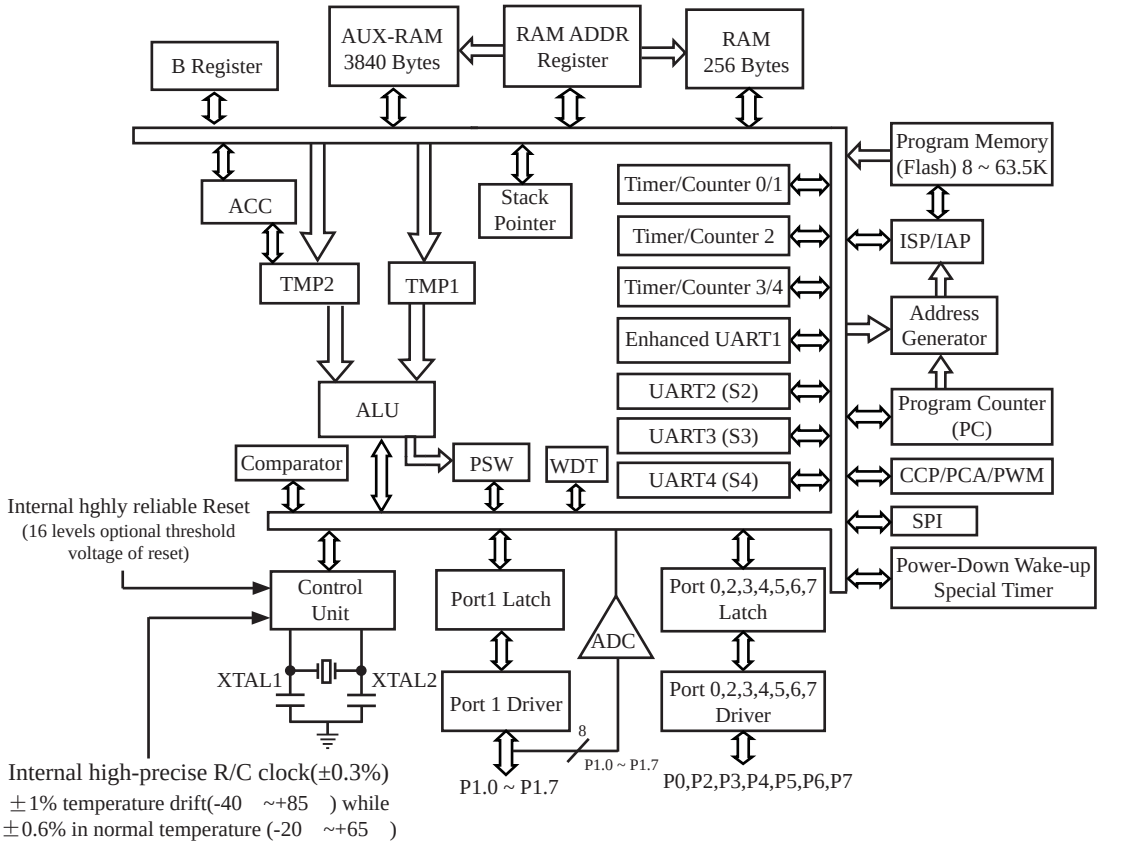
- Comparator, which can be used as 1 channel ADC or brownout detect function and support comparing by external pin CMP+ and CMP- or internal reference voltage and generating output signal (its polarity can be configured) on CMPO pin.
- One 15 bits Watch-Dog-Timer with 8-bit pre-scaler (one-time-enabled)
- advanced instruction set, which is fully compatible with traditional 8051 MCU, have hardware multiplication / division command.
- 62/46/42/38/30/26 common I/O ports are available, their mode is quasi_bidirectional/weak pull-up (traditional 8051 I/O ports mode) after reset, and can be set to four modes: quasi_bidirectional/weak pull-up, strong push-pull/ strong pull-up, input-only/high-impedance and open drain.

  the driving ability of each I/O port can be up to 20mA, but it don't exceed this maximum 120mA that the current of the whole chip of 40-pin or more than 40-pin MCU, while 90mA that the current of the whole chip of 16-pin or more than 16-pin MCU or 32-pin or less than 32-pin MCU.

  If I/O ports are not enough, it can be extended by connecting a 74HC595(reference price: RMB 0.21 yuan). Besides, cascading several chips also can extend to dozens of I/O ports.
- Package: LQFP64L(16mm x 16mm), LQFP64S(12mm x 12mm), LQFP48(9mm x 9mm), LQFP44(12mm x 12mm), LQFP32(9mm x 9mm), SOP28, SKDIP28, PDIP40.
- All products are baked 8 hours in high-temperature 175 after be packaged, Manufacture guarantee good quality.
- In Keil C development environment, select the Intel 8052 to compiling and only contain < reg51.h > as header file.

2. Block diagram of STC15W4K32S4 series MCU

The internal structure of STC15W4K32S4 series MCU is shown in the block diagram below. STC15W4K32S4 series MCU includes central processor unit(CPU), program memory (Flash), data memory(SRAM), Timers/Counters, I/O ports, high-speed A/D converter(ADC), Comparator,Watchdog, high-speed asynchronous serial communication ports---UART(UART1/UART2/UART3/UART4), CCP/PWM/PCA, a group of high-speed synchronous serial peripheral interface (SPI), internal high- precise R/C clock, internal hghly reliable Reset and so on. STC15W4K32S4 series MCU almost includes all of the modules required in data acquisition and control, so can be regarded as an on-chip system (SysTem Chip or SysTem on Chip, abbreviated as STC, this is the name origin of Hongjing technology STC Limited).

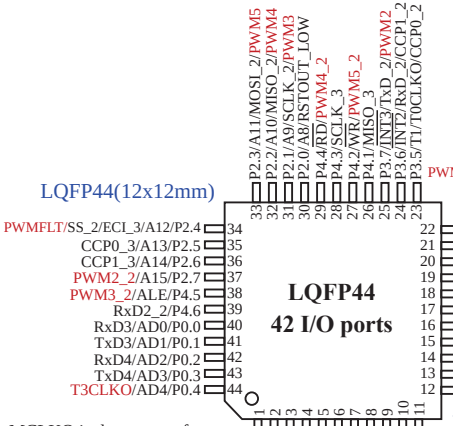


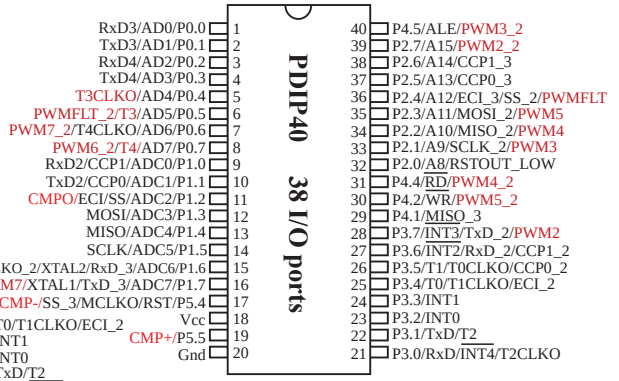
STC15W4K32S4 series Block Diagram

3. Pin Configurations of STC15W4K32S4 series MCU

All packages meet EU RoHS standards

CCP is abbreviation for Capture, Compare, PWM



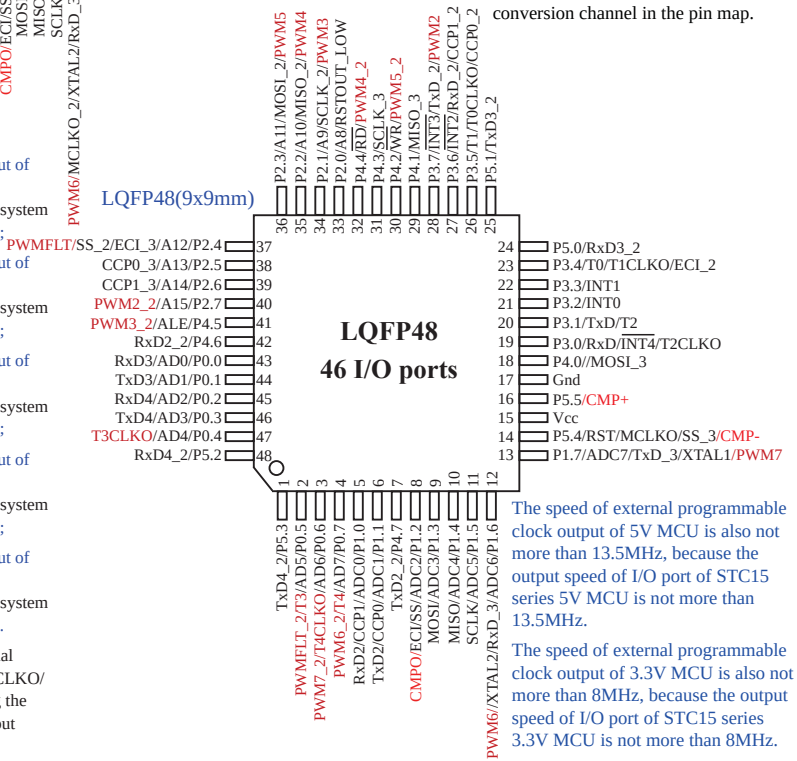


Note P0 ports can be multiplexed as Address/Data bus not as A/D Converter. 8 channels of A/D Converter are on P1.

Consequently P0.x/ADx means that P0.x can be used as Address/ Data bus, while P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.

Recommend UART1 on [P3.6/RxD_2, P3.7/TxD_2] or [P1.6/RxD_3/XTAL2, P1.7/TxD_3/XTAL1]

MCLKO is the output of master clock whose frequency can be divided into MCLK/**1,** MCLK/2, MCLK/4, MCLK/16 The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator. MCLK is the frequency of master clock.



T0CLKO refers to the programmable clock output of Timer/Counter 0
(output by dividing the frequency of the internal system clock or the input clock of external pin T0/P3.4);

T1CLKO refers to the programmable clock output of Timer/Counter 1
(output by dividing the frequency of the internal system clock or the input clock of external pin T1/P3.5);

T2CLKO refers to the programmable clock output of Timer/Counter 2
(output by dividing the frequency of the internal system clock or the input clock of external pin T2/P3.1);

T3CLKO refers to the programmable clock output of Timer/Counter 3
(output by dividing the frequency of the internal system clock or the input clock of external pin T3/P0.5);

T4CLKO refers to the programmable clock output of Timer/Counter 4
(output by dividing the frequency of the internal system clock or the input clock of external pin T4/P0.7).

In addition to programmable output on the internal system clock, T0CLKO/T1CLKO/T2CLKO/T3CLKO/ T4CLKO also can be used as divider by dividing the frequency of the internal system clock or the input clock of external pin T0/T1/T2/T3/T4.

The speed of external programmable clock output of 5V MCU is also not more than 13.5MHz, because the output speed of I/O port of STC15 series 5V MCU is not more than 13.5MHz.

The speed of external programmable clock output of 3.3V MCU is also not more than 8MHz, because the output speed of I/O port of STC15 series 3.3V MCU is not more than 8MHz.

T0CLKO refers to the programmable clock output of Timer/Counter 0 (output by dividing the frequency of the internal system clock or the input clock of external pin T0/P3.4);

T1CLKO refers to the programmable clock output of Timer/Counter 1 (output by dividing the frequency of the internal system clock or the input clock of external pin T1/P3.5);

T2CLKO refers to the programmable clock output of Timer/Counter 2 (output by dividing the frequency of the internal system clock or the input clock of external pin T2/P3.1);

T3CLKO refers to the programmable clock output of Timer/Counter 3 (output by dividing the frequency of the internal system clock or the input clock of external pin T3/P0.5);

T4CLKO refers to the programmable clock output of Timer/Counter 4 (output by dividing the frequency of the internal system clock or the input clock of external pin T4/P0.7).

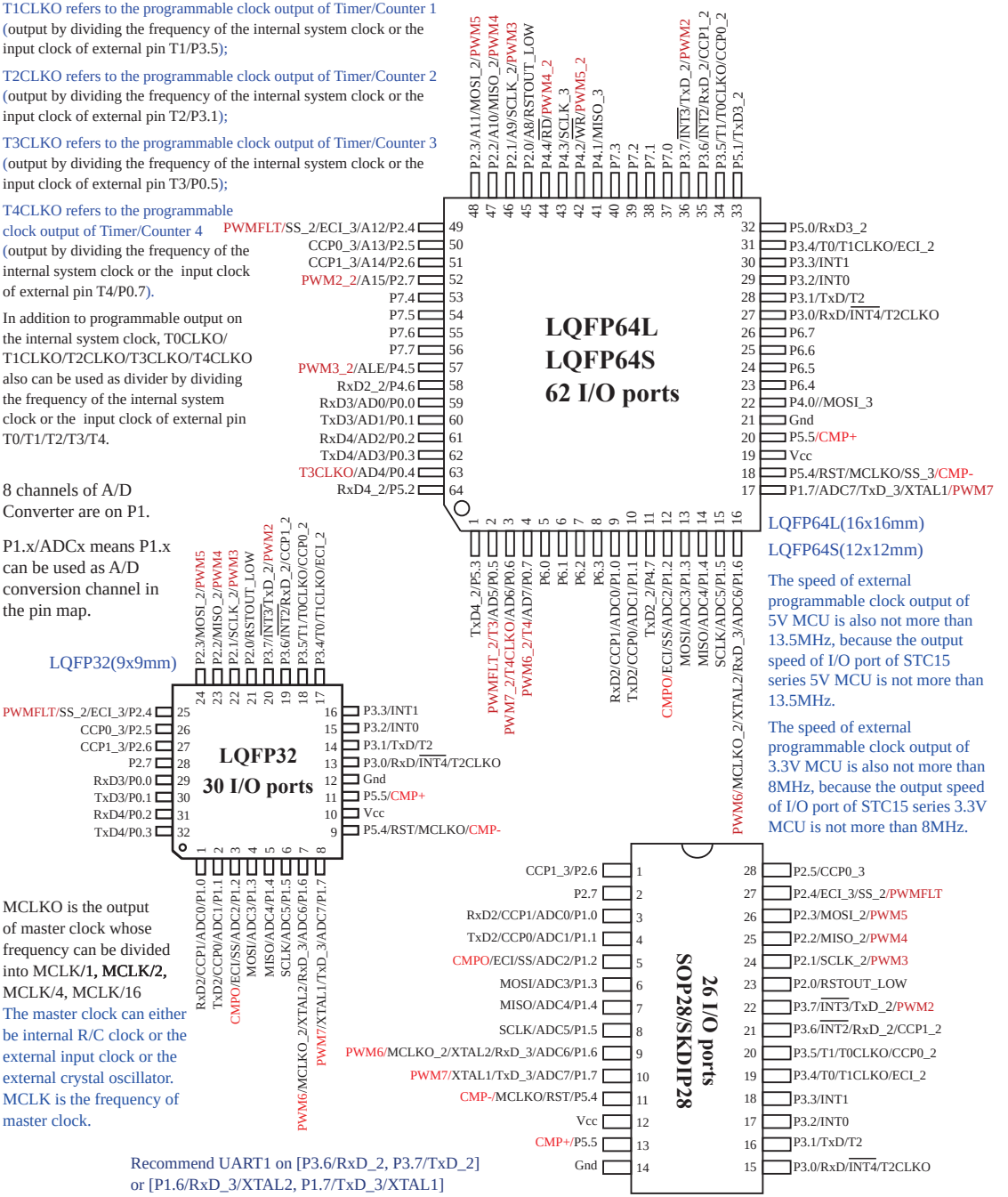
In addition to programmable output on the internal system clock, T0CLKO/T1CLKO/T2CLKO/T3CLKO/T4CLKO also can be used as divider by dividing the frequency of the internal system clock or the input clock of external pin T0/T1/T2/T3/T4.

8 channels of A/D Converter are on P1.

P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.

All packages meet EU RoHS standards

CCP is abbreviation for Capture, Compare, PWM



LQFP64L(16x16mm)

LQFP64S(12x12mm)

The speed of external programmable clock output of 5V MCU is also not more than 13.5MHz, because the output speed of I/O port of STC15 series 5V MCU is not more than 13.5MHz.

The speed of external programmable clock output of 3.3V MCU is also not more than 8MHz, because the output speed of I/O port of STC15 series 3.3V MCU is not more than 8MHz.

LQFP32(9x9mm)

MCLKO is the output of master clock whose frequency can be divided into MCLK/1, MCLK/2, MCLK/4, MCLK/16

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator. MCLK is the frequency of master clock.

Recommend UART1 on [P3.6/RxD_2, P3.7/TxD_2] or [P1.6/RxD_3/XTAL2, P1.7/TxD_3/XTAL1]

Mnemonic	Add	Name	7	6	5	4	3	2	1	0	Reset Value
AUXR1 P_SW1	A2H	Auxiliary register 1	S1_S1	S1_S0	CCP_S1	CCP_S0	SPI_S1	SPI_S0	0	DPS	0000 0000
P_SW2	BAH	Peripheral function switch			PWM67_S	PWM2345_S		S4_S	S3_S	S2_S	xxxx x000
CLK_DIV (PCON2)	97H	Clock Division register	MCKO_S1	MCKO_S0	ADRJ	Tx_Rx	MCLKO_2	CLKS2	CLKS1	CLKS0	0000 0000
INT_CLKO (AUXR2)	8FH	External Interrupt enable and Clock output register	-	EX4	EX3	EX2	MCKO_S2	T2CLKO	T1CLKO	T0CLKO	x000 0000

UART1/S1 can be switched in 3 groups of pins by selecting the control bits S1_S0 and S1_S1.		
S1_S1	S1_S0	UART1/S1 can be switched between P1 and P3
0	0	UART1/S1 on [P3.0/RxD,P3.1/TxD]
0	1	UART1/S1 on [P3.6/RxD_2,P3.7/TxD_2]
1	0	UART1/S1 on [P1.6/RxD_3/XTAL2,P1.7/TxD_3/XTAL1] when UART1 is on P1, please using internal R/C clock.
1	1	Invalid

Recommed UART1 on [P3.6/RxD_2,P3.7/TxD_2] or [P1.6/RxD_3/XTAL2,P1.7/TxD_3/XTAL1].

UART2/S2 can be switched in 2 groups of pins by selecting the control bit S2_S.	
S2_S	UART2/S2 can be switched between P1 and P4
0	UART2/S2 on [P1.0/RxD2,P1.1/TxD2]
1	UART2/S2 on [P4.6/RxD2_2,P4.7/TxD2_2]

UART3/S3 can be switched in 2 groups of pins by selecting the control bit S3_S.	
S3_S	UART3/S3 can be switched between P0 and P5
0	UART3/S3 on [P0.0/RxD3,P0.1/TxD3]
1	UART3/S3 on [P5.0/RxD3_2,P5.1/TxD3_2]

UART4/S4 can be switched in 2 groups of pins by selecting the control bit S4_S.	
S4_S	UART4/S4 can be switched between P0 and P5
0	UART4/S4 on [P0.2/RxD4,P0.3/TxD4]
1	UART4/S4 on [P5.2/RxD4_2,P5.3/TxD4_2]

SPI can be switched in 3 groups of pins by selecting the control bits SPI_S1 and SPI_S0		
SPI_S1	SPI_S0	SPI can be switched in P1 and P2 and P4
0	0	SPI on [P1.2/SS,P1.3/MOSI,P1.4/MISO,P1.5/SCLK]
0	1	SPI on [P2.4/SS_2,P2.3/MOSI_2,P2.2/MISO_2,P2.1/SCLK_2]
1	0	SPI on [P5.4/SS_3,P4.0/MOSI_3,P4.1/MISO_3,P4.3/SCLK_3]
1	1	Invalid

Mnemonic	Add	Name	7	6	5	4	3	2	1	0	Reset Value
AUXR1 P_SW1	A2H	Auxiliary register 1	S1_S1	S1_S0	CCP_S1	CCP_S0	SPI_S1	SPI_S0	0	DPS	0000 0000
P_SW2	BAH	Peripheral function switch			PWM67_S	PWM2345_S		S4_S	S3_S	S2_S	xxxx x000
CLK_DIV (PCON2)	97H	Clock Division register	MCKO_S1	MCKO_S0	ADRJ	Tx_Rx	MCLKO_2	CLKS2	CLKS1	CLKS0	0000 0000

CCP can be switched in 3 groups of pins by selecting the control bits CCP_S1 and CCP_S0.		
CCP_S1	CCP_S0	CCP can be switched in P1 and P2 and P3
0	0	CCP on [P1.2/ECI,P1.1/CCP0,P1.0/CCP1]
0	1	CCP on [P3.4/ECI_2,P3.5/CCP0_2,P3.6/CCP1_2]
1	0	CCP on [P2.4/ECI_3,P2.5/CCP0_3,P2.6/CCP1_3]
1	1	Invalid

PWM2/PWM3/PWM4/PWM5/PWMFLT can be switched in 2 groups of pins by selecting the control bit PWM2345_S.	
PWM2345_S	PWM2/PWM3/PWM4/PWM5/PWMFLT can be switched between P2, P3, and P4
0	PWM2/PWM3/PWM4/PWM5/PWMFLT on [P3.7/PWM2, P2.1/PWM3, P2.2/PWM4, P2.3/PWM5, P2.4/PWMFLT]
1	PWM2/PWM3/PWM4/PWM5/PWMFLT on [P2.7/PWM2_2, P4.5/PWM3_2, P4.4/ PWM4_2, P4.2/PWM5_2, P0.5/PWMFLT_2]

PWM6/PWM7 can be switched in 2 groups of pins by selecting the control bit PWM67_S.	
PWM67_S	PWM2/PWM3/PWM4/PWM5/PWMFLT can be switched between P0 and P1
0	PWM6/PWM7 on [P1.6/PWM6,P1.7/PWM7]
1	PWM6/PWM7 on [P0.7/PWM6_2,P0.6/PWM7_2]

DPS DPTR registers select bit.

0 DPTR0 is selected

1 DPTR1 is selected

ADRJ the adjustment bit of ADC result

0 ADC_RES[7:0] store high 8-bit ADC result ADC_RESL[1:0] store low 2-bit ADC result

1 ADC_RES[1:0] store high 2-bit ADC result ADC_RESL[7:0] store low 8-bit ADC result

Tx_Rx the set bit of relay and broadcast mode of UART1

0 UART1 works on normal mode

1 UART1 works on relay and broadcast mode that to say output the input level state of RxD port to the outside TxD pin in real time, namely the external output of TxD pin can reflect the input level state of RxD port.

the RxD and TxD of UART1 can be switched in 3 groups of pins: [RxD/P3.0, TxD/P3.1];
[RxD_2/P3.6, TxD_2/P3.7];
[RxD_3/P1.6, TxD_3/P1.7].

Mnemonic	Add	Name	7	6	5	4	3	2	1	0	Reset Value
CLK_DIV (PCON2)	97H	Clock Division register	MCKO_S1	MCKO_S0	ADRJ	Tx_Rx	MCLKO_2	CLKS2	CLKS1	CLKS0	0000 0000
INT_CLKO (AUXR2)	8FH	External Interrupt enable and Clock output register	-	EX4	EX3	EX2	MCKO_S2	T2CLKO	T1CLKO	T0CLKO	x000 0000

MCKO_S2	MCKO_S1	MCKO_S0	the control bit of master clock output by dividing the frequency (The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator)
0	0	0	Master clock do not output external clock
0	0	1	Master clock output external clock but its frequency do not be divided and the output clock frequency = MCLK / 1
0	1	0	Master clock output external clock but its frequency is divided by 2 and the output clock frequency = MCLK / 2
0	1	1	Master clock output external clock but its frequency is divided by 4 and the output clock frequency = MCLK / 4
1	0	0	Master clock output external clock but its frequency is divided by 4 and the output clock frequency = MCLK / 16

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.
MCLK is the frequency of master clock.
STC15W4K32S4 series MCU output master clock on MCLKO/P5.4

MCLKO_2 to select Master Clock output on where
- 0 Master Clock output on MCLKO/P5.4
- 1 Master Clock output on MCLKO_2/XTAL2/P1.6

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.

CLKS2	CLKS1	CLKS0	the control bit of system clock (System clock refers to the master clock that has been divided frequency, which is offered to CPU, UARTs, SPI, Timers, CCP/PWM/PCA and A/D Converter)
0	0	0	Master clock frequency/1, No division
0	0	1	Master clock frequency/2
0	1	0	Master clock frequency/4
0	1	1	Master clock frequency/8
1	0	0	Master clock frequency/16
1	0	1	Master clock frequency/32
1	1	0	Master clock frequency/64
1	1	1	Master clock frequency/128

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.

4. STC15W4K32S4 series Selection and Price Table

Type 1T 8051 MCU	Operating Voltage (V)	Flash (byte)	SRAM (byte)	UART	SPI	common Timers T0-T4	8 channels PWM: 15-bit special PWM (with a dead-section controller)	8 channels PWM: 10-bit CCP	Speical Power-down Wake-up Timer	Standard External Interrupts	A/D 8-channel	COMPARATOR	DPTR	EEPROM	Internal Low-Voltage Detection Interrupt	WDT	Internal High-reliable Reset (with optional threshold voltage)	Internal High-Precise Clock	Output clock and reset signal from MCU	Encryption Download (to protect your code from being intercepted)	RS485 Control	All Packages LQFP64/LQFP48/LQFP44/PDIP40 LQFP32/SOP28/SKDIP28 Price of a part of packages (RMB ¥): PDIP 40	LQFP 44	LQFP 48	LQFP 64S
STC15W4K32S4 series MCU Selection and Price Table Note: 8 channels PWM can be used as 8 channels DAC, 2 channels CCP can be used as 2 Timers or 2 external interrupts.																									
STC15W4K16S4	5.5-2.5	16K	4K	4	Y	5	6-ch	2-ch	Y	5	10 bits	Y	2	45K	Y	Y	16-level	Y	Y	Y	Y	¥5.7	¥5.2	¥5.2	¥5.4
STC15W4K32S4	5.5-2.5	32K	4K	4	Y	5	6-ch	2-ch	Y	5	10 bits	Y	2	29K	Y	Y	16-level	Y	Y	Y	Y	¥5.9	¥5.5	¥5.5	¥5.7
STC15W4K40S4	5.5-2.5	40K	4K	4	Y	5	6-ch	2-ch	Y	5	10 bits	Y	2	21K	Y	Y	16-level	Y	Y	Y	Y	¥5.9	¥5.6	¥5.6	¥5.8
STC15W4K48S4	5.5-2.5	48K	4K	4	Y	5	6-ch	2-ch	Y	5	10 bits	Y	2	13K	Y	Y	16-level	Y	Y	Y	Y	¥5.9	¥5.6	¥5.6	¥5.8
STC15W4K56S4	5.5-2.5	56K	4K	4	Y	5	6-ch	2-ch	Y	5	10 bits	Y	2	5K	Y	Y	16-level	Y	Y	Y	Y	¥5.9	¥5.6	¥5.6	¥5.8
IAP15W4K58S4 (which itself is a emluator)	5.5-2.5	58K	4K	4	Y	5	6-ch	2-ch	Y	5	10 bits	Y	2	IAP	Y	Y	16-level	Y	Y	Y	Y	¥5.9	¥5.6	¥5.6	¥5.8
																						The program Flash in user program area can be used as EEPROM.			
IAP15W4K61S4 (which itself is a emluator)	5.5-2.5	61K	4K	4	Y	5	6-ch	2-ch	Y	5	10 bits	Y	2	IAP	Y	Y	16-level	Y	Y	Y	Y	¥5.9	¥5.6	¥5.6	¥5.8
																						The program Flash in user program area can be used as EEPROM.			
IRC15W4K63S4 (Using external crystal or internal 24MHz clock)	5.5-2.5	63.5K	4K	4	Y	5	6-ch	2-ch	Y	5	10 bits	Y	2	IAP	Y	Y	Fixed	Y	Y	N	N	¥5.9	¥5.6	¥5.6	¥5.8
																						The program Flash in user program area can be used as EEPROM.			

Encryption Download : please burn source code with encryption key onto MCU in the factory. Then, you can make a simple update software just with one "update" button by fisrtly using the fuction "encrytion download" and then "release project" to update yourself code unabled to be intercepted when you need to upgrade your code.

If user wants to use 40-pin and above MCU, LQFP-44 is suggested, while PDIP-40 is still supplied normal ; if user wants to use the 32-pin MCU, LQFP-32 is recommeded; if user wants to use the 28-pin MCU, SOP-28 is recommended.

To provide customized IC services

Because the last 7 bytes of the program area is stored mandatorily the contents of only global ID, the program space the user can actually use is 7 bytes smaller than the space shown in the selection table.

Conclusion : STC15W4K32S4 series MCU have: Five 16-bit relaodable Timers/Counters that are Timer/Counter 0, Timer/Counter 1, Timer/Counter 2, Timer/Counter 3 and Timer/Counter 4; 8 channels and 10 bits PWM (can achieve 8 D/A converters or 2 timers or 2 external interrupts again); special power-down wake-up timer; 5 external interrupts INT0/INT1/$\overline{\text{INT2}}$/$\overline{\text{INT3}}$/$\overline{\text{INT4}}$; 4 high-speed asynchronous serial ports ---- UARTs (UART1/UART2/UART3/UART4 can be used simultaneously); a high-speed synchronous serial peripheral interface ---- SPI; 8 channels and 10 bits high-speed A/D converter; a group of Comparator, 2 data pointers ---- DPTR; external data bus and so on.

5. Naming rules of STC15W4K32S4 series MCU

xxx 15 x 4K xx xx -- 35 x - xxxxx xx

Pin Number
e.g. 64, 48, 44, 40, 32, 28

Package type
e.g. LQFP, PDIP, SOP, SKDIP

Temperature range
I : Industrial, -40 -85
C : Commercial, 0 -70

Operating frequency
35 : Up to 35MHz

S4 4 UARTs (can be used simultaneously)
SPI
Internal EEPROM
A/D Converter(PWM also can be used as DAC)
CCP/PWM/PCA

Program space, e.g.
08:8KB 16:16KB 24:24KB 32:32KB 48:48KB 56:56KB
58:58KB 61:61KB 63:63.5KB etc.

SRAM: 4K = 4096 bytes

Operating Voltage
W : 5.5V ~ 2.5V

STC 1T 8051 MCU,
Speed is 8~12 times faster than the traditional 8051 in the same working frequency

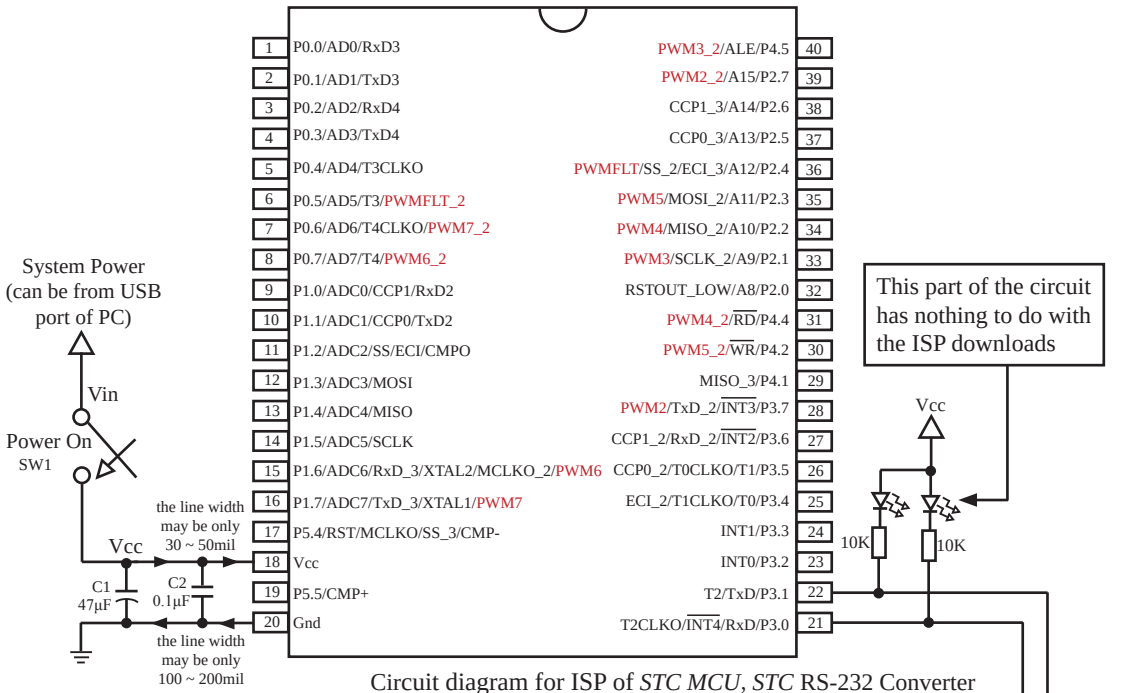
STC : The program Flash in user program area can not be used as EEPROM., but there are special EEPROM.

IAP : The program Flash in user program area can be used as EEPROM.

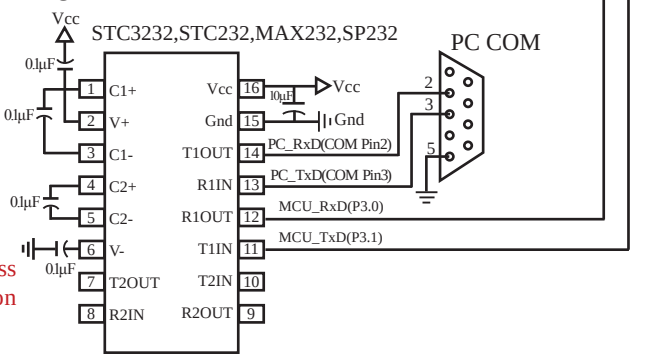
IRC : The program Flash in user program area can be used as EEPROM, and to use external crystal or internal 24MHz clock

6. Application Circuit Diagram for ISP of STC15W4K series

6.1 Application Circuit Diagram for ISP using RS-232 Converter



Circuit diagram for ISP of *STC MCU*, *STC* RS-232 Converter



Note P0 ports can be multiplexed as Address/Data bus not as A/D Converter. 8 channels of A/D Converter are on P1.

Consequently P0.x/ADx means that P0.x can be used as Address/Data bus, while P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.

Please power on the target MCU after press down the button "Download/Program" on STC-ISP.exe when burning code to MCU.

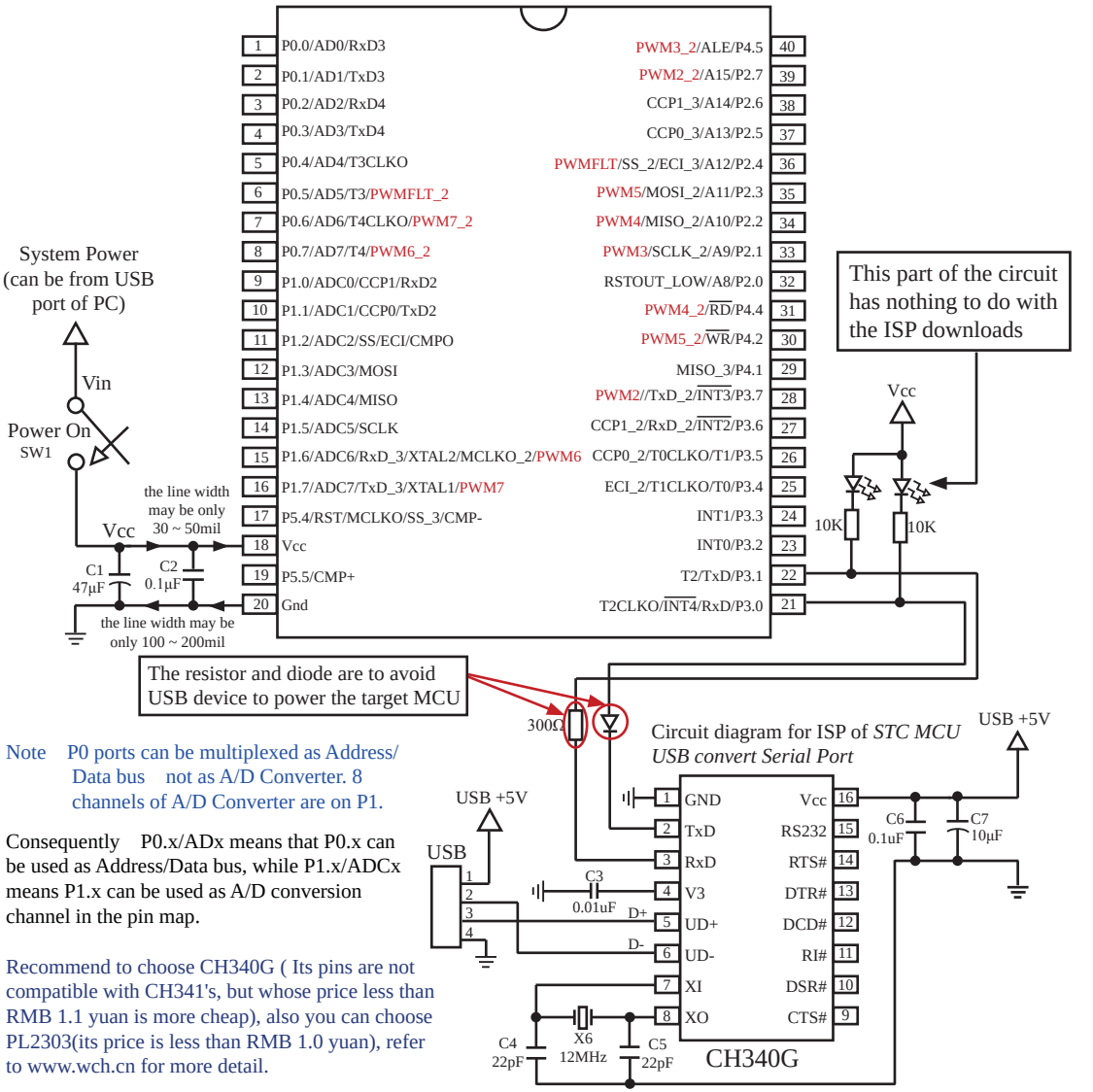
Internal hghly reliable Reset, so external reset circuit can be completely removed.

P5.4/RST/MCLKO pin factory defaults to the I/O port, which can be set as RST reset pin(active high) through the STC-ISP programmer.

Internal high-precise R/C clock(±3%), ±1% temperature drift (-40 ~+85) while ±0.6% in normal temperature (-20 ~+65), so external expensive crysal can be completely removed.

Recommend to add decoupling capacitor C1(47μF) and C2(0.1μF) between Vcc and Gnd that can remove power noise and improve the anti-interference ability.

6.2 Application Circuit Diagram for ISP using USB to convert Serial



Note P0 ports can be multiplexed as Address/Data bus not as A/D Converter. 8 channels of A/D Converter are on P1.

Consequently P0.x/ADx means that P0.x can be used as Address/Data bus, while P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.

Recommend to choose CH340G (Its pins are not compatible with CH341's, but whose price less than RMB 1.1 yuan is more cheap), also you can choose PL2303(its price is less than RMB 1.0 yuan), refer to www.wch.cn for more detail.

Internal hghly reliable Reset, so external reset circuit can be completely removed.

P5.4/RST/MCLKO pin factory defaults to the I/O port, which can be set as RST reset pin(active high) through the STC-ISP programmer.

Internal high-precise R/C clock(±3%), ±1% temperature drift (-40 ~+85) while ±0.6% in normal temperature (-20 ~+65), so external expensive crysal can be completely removed.

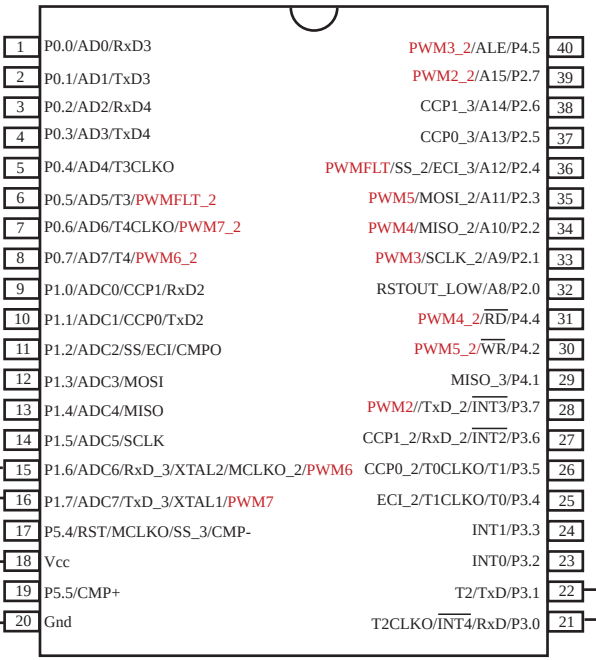
Recommend to add decoupling capacitor C1(47μF) and C2(0.1μF) between Vcc and Gnd that can remove power noise and improve the anti-interference ability.

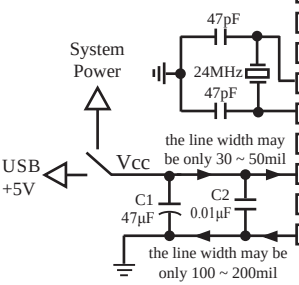
6.3 Application Circuit Diagram for ISP directly using USB port

——P3.0/P3.1 of STC15W4K series and IAP15W4K58S4 connect directly with D-/D+ of USB

Note P0 ports can be multiplexed as Address/Data bus not as A/D Converter. 8 channels of A/D Converter are on P1.

Consequently P0.x/ADx means that P0.x can be used as Address/Data bus, while P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.

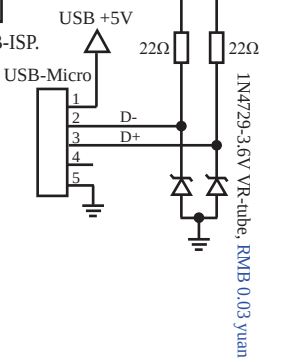




The MCU can be powered by USB port or system power

Application Circuit Diagram for ISP directly using USB port, USB-ISP. MCU P3.0/P3.1 connect directly with D-/D+ of USB

The Application Circuit Diagram applies to STC15W4K series and IAP15W4K58S4 MCU only.



USB-Micro

7. Pin Descriptions of STC15W4K32S4 series MCU

MNEMONIC	Pin Number							DESCRIPTION	
	LQFP64	LQFP48	LQFP44	PDIP40	SOP32	LQFP32	SOP28 SKDIP28		
P0.0/AD0/ RxD3	59	43	40	1	1	29	-	P0.0	common I/O port PORT0[0]
								AD0	Address/Data Bus
								RxD3	Receive Data Port of UART3
P0.1/AD1/ TxD3	60	44	41	2	2	30	-	P0.1	common I/O port PORT0[1]
								AD1	Address/Data Bus
								TxD3	Transit Data Port of UART3
P0.2/AD2/ RxD4	61	45	42	3	3	31	-	P0.2	common I/O port PORT0[2]
								AD2	Address/Data Bus
								RxD4	Receive Data Port of UART4
P0.3/AD3/ TxD4	62	46	43	4	4	32	-	P0.3	common I/O port PORT0[3]
								AD3	Address/Data Bus
								TxD4	Transit Data Port of UART4
P0.4/AD4/ T3CLKO	63	47	44	5	-	-	-	P0.4	common I/O port PORT0[4]
								AD4	Address/Data Bus
								T3CLKO	T3 Clock Output The pin can be configured for T3CLKO by setting T4T3M[0] bit /T3CLKO
P0.5/AD5/T3/ PWMFLT_2	2	2	1	6	-	-	-	P0.5	common I/O port PORT0[5]
								AD5	Address/Data Bus
								T3	External input of Timer/Counter 3
								PWMFLT_2	Control PWM to emergency stop
P0.6/AD6/ T4CLKO/ PWM7_2	3	3	2	7	-	-	-	P0.6	common I/O port PORT0[6]
								AD6	Address/Data Bus
								T4CLKO	T4 Clock Output The pin can be configured for T4CLKO by setting T4T3M[4] bit /T4CLKO
								PWM7_2	The seventh output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P0.7/AD7/T4/ PWM6_2	4	4	3	8	-	-	-	P0.7	common I/O port PORT0[7]
								AD7	Address/Data Bus
								T4	External input of Timer/Counter 4
								PWM6_2	The sixth output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P1.0/ADC0/ CCP1/RxD2	9	5	4	9	5	1	3	P1.0	common I/O port PORT1[0]
								ADC0	ADC input channel-0
								CCP1	Capture of external signal(measure frequency or be used as external interrupts) high-speed Pulse and Pulse-Width Modulation output channel-1
								RxD2	Receive Data Port of UART2

MNEMONIC	Pin Number							DESCRIPTION	
	LQFP64	LQFP48	LQFP44	PDIP40	SOP32	LQFP32	SOP28 SKDIP28		
P1.1/ADC1/ CCP0/TxD2	10	6	5	10	6	2	4	P1.1	common I/O port PORT1[1]
								ADC1	ADC input channel-1
								CCP0	Capture of external signal(measure frequency or be used as external interrupts) high-speed Pulse and Pulse-Width Modulation output channel-0
								TxD2	Transit Data Port of UART2
P1.2/ADC2/ SS/ECI/ CMPO	12	8	7	11	7	3	5	P1.2	common I/O port PORT1[2]
								ADC2	ADC input channel-2
								SS	Slave selection signal of synchronous serial peripheral interface----SPI
								ECI	External pulse input pin of CCP/ PCA counter
								CMPO	The output port of reslut compared by comparator
P1.3/ADC3/ MOSI	13	9	8	12	8	4	6	P1.3	common I/O port PORT1[3]
								ADC3	ADC input channel-3
								MOSI	Master Output Slave Input of SPI
P1.4/ADC4/ MISO	14	10	9	13	9	5	7	P1.4	common I/O port PORT1[4]
								ADC4	ADC input channel-4
								MISO	Master Iutput Slave Onput of SPI
P1.5/ADC5/ SCLK	15	11	10	14	10	6	8	P1.5	common I/O port PORT1[5]
								ADC5	ADC input channel-5
								SCLK	Clock Signal of synchronous serial peripheral interface----SPI
P1.6/ADC6/ RxD_3/ XTAL2/ MCLKO_2/ PWM6	16	12	11	15	11	7	9	P1.6	common I/O port PORT1[6]
								ADC6	ADC input channel--6
								RxD_3	Receive Data Port of UART1
								MCLKO_2	Master clock output; the output frequency can be MCLK/1, MCLK/2 and MCLK/4. The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.
								XTAL2	Output from the inverting amplifier of internal clock circuit. This pin should be floated when an external oscillator is used.
								PWM6	The sixth output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset

MNEMONIC	Pin Number							DESCRIPTION	
	LQFP64	LQFP48	LQFP44	PDIP40	SOP32	LQFP32	SOP28 SKDIP28		
P1.7/ADC7/ TxD_3/ XTAL1/ PWM7	17	13	12	16	12	8	10	P1.7	common I/O port PORT1[7]
								ADC7	ADC input channel--7
								TxD_3	Transit Data Port of UART1
								XTAL1	Input to the inverting oscillator amplifier of internal clock circuit. Receives the external oscillator signal when an external oscillator is used.
								PWM7	The seventh output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P2.0/A8/ RSTOUT_LOW	45	33	30	32	25	21	23	P2.0	common I/O port PORT2[0]
								A8	The eighth bit of Address bus — A8
								RSTOUT_LOW	the pin output low after power-on and during reset, which can be set to output high by software
P2.1/A9/ SCLK_2/ PWM3	46	34	31	33	26	22	24	P2.1	common I/O port PORT2[1]
								A9	The ninth bit of Address bus — A9
								SCLK_2	Clock Signal of synchronous serial peripheral interface----SPI
								PWM3	The third output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P2.2/A10/ MISO_2/ PWM4	47	35	32	34	27	23	25	P2.2	common I/O port PORT2[2]
								A10	The tenth bit of Address bus — A10
								MISO_2	Master Iutput Slave Onput of SPI
								PWM4	The fourth output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P2.3/A11/ MOSI_2/ PWM5	48	36	33	35	28	24	26	P2.3	common I/O port PORT2[3]
								A11	The eleventh bit of Address bus —A11
								MOSI_2	Master Output Slave Input of SPI
								PWM5	The fifth output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P2.4/A12/ ECI_3/SS_2/ PWMFLT	49	37	34	36	29	25	27	P2.4	common I/O port PORT2[4]
								A12	The twelfth bit of Address bus — A12
								ECI_3	External pulse input pin of CCP/PCA counter
								SS_2	Slave selection signal of synchronous serial peripheral interface----SPI
								PWMFLT	Control PWM to emergency stop
P2.5/A13/ CCP0_3	50	38	35	37	30	26	28	P2.5	common I/O port PORT2[5]
								A13	The thirteenth bit of Address bus — A13
								CCP0_3	Capture of external signal(measure frequency or be used as external interrupts) high-speed Pulse and Pulse-Width Modulation output channel-0

MNEMONIC	Pin Number							DESCRIPTION	
	LQFP64	LQFP48	LQFP44	PDIP40	SOP32	LQFP32	SOP28 SKDIP28		
P2.6/A14/ CCP1_3	51	39	36	38	31	27	1	P2.6	common I/O port PORT2[6]
								A14	The fourteenth bit of Address bus—A14
								CCP1_3	Capture of external signal(measure frequency or be used as external interrupts) high-speed Pulse and Pulse-Width Modulation output channel-1
P2.7/A15/ PWM2_2	52	40	37	39	32	28	2	P2.7	common I/O port PORT2[7]
								A15	The fifteenth bit of Address bus — A15
								PWM2_2	The second output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P3.0/RxD/ $\overline{\text{INT4}}$ /T2CLKO	27	19	18	21	17	13	15	P3.0	common I/O port PORT3[0]
								RxD	Receive Data Port of UART1
								$\overline{\text{INT4}}$	External interrupt 4, which only can be generated on falling edge. /INT4 supports power-down waking-up
								T2CLKO	T2 Clock Output The pin can be configured for T2CLKO by setting INT_CLKO[2] bit /T2CLKO
P3.1/TxD/T2	28	20	19	22	18	14	16	P3.1	common I/O port PORT3[1]
								TxD	Transit Data Port of UART1
								T2	External input of Timer/Counter 2
P3.2/INT0	29	21	20	23	19	15	17	P3.2	common I/O port PORT3[2]
								INT0	External interrupt 0, which both can be generated on rising and falling edge. INT0 only can generate interrupt on falling edge if IT0 (TCON.0) is set to 1. And, INT0 both can generate interrupt on rising and falling edge if IT0 (TCON.0) is set to 0.
P3.3/INT1	30	22	21	24	20	16	18	P3.3	common I/O port PORT3[3]
								INT1	External interrupt 1, which both can be generated on rising and falling edge. INT1 only can generate interrupt on falling edge if IT1 (TCON.2) is set to 1. And, INT1 both can generate interrupt on rising and falling edge if IT1 (TCON.2) is set to 0. INT1 supports power-down waking-up
P3.4/T0/ T1CLKO/ ECI_2	31	23	22	25	21	17	19	P3.4	common I/O port PORT3[4]
								T0	External input of Timer/Counter 0
								T1CLKO	T1 Clock Output The pin can be configured for T1CLKO by setting INT_CLKO[1] bit /T1CLKO
								ECI_2	External pulse input pin of CCP/PCA counter

MNEMONIC	Pin Number							DESCRIPTION	
	LQFP64	LQFP48	LQFP44	PDIP40	SOP32	LQFP32	SOP28 SKDIP28		
P3.5/T1/ T0CLKO/ CCP0_2	34	26	23	26	22	18	20	P3.5	common I/O port PORT3[5]
								T1	External input of Timer/Counter 1
								T0CLKO	T0 Clock Output The pin can be configured for T0CLKO by setting INT_CLKO[0] bit /T0CLKO
								CCP0_2	Capture of external signal(measure frequency or be used as external interrupts) high-speed Pulse and Pulse-Width Modulation output channel-0
P3.6/$\overline{\text{INT2}}$/ RxD_2/ CCP1_2	35	27	24	27	23	19	21	P3.6	common I/O port PORT3[6]
								$\overline{\text{INT2}}$	External interrupt 2, which only can be generated on falling edge. /INT2 supports power-down waking-up
								RxD_2	Receive Data Port of UART1
								CCP1_2	Capture of external signal(measure frequency or be used as external interrupts) high-speed Pulse and Pulse-Width Modulation output channel-1
P3.7/$\overline{\text{INT3}}$ /TxD_2/ PWM2	36	28	25	28	24	20	22	P3.7	common I/O port PORT3[7]
								$\overline{\text{INT3}}$	External interrupt 3, which only can be generated on falling edge. /INT3 supports power-down waking-up
								TxD_2	Transit Data Port of UART1
								PWM2	The second output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P4.0/MOSI_3	22	18	17	-	-	-	-	P4.0	common I/O port PORT4[0]
								MISO_3	Master Iutput Slave Onput of SPI
P4.1/MISO_3	41	29	26	29	-	-	-	P4.1	common I/O port PORT4[1]
								MOSI_3	Master Output Slave Input of SPI
P4.2/$\overline{\text{WR}}$ /PWM5_2	42	30	27	30	-	-	-	P4.2	common I/O port PORT4[2]
								$\overline{\text{WR}}$	Write pulse of external data memory
								PWM5_2	The fifth output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P4.3/SCLK_3	43	31	28	-	-	-	-	P4.3	PORT4[3]
								SCLK_3	Clock Signal of synchronous serial peripheral interface----SPI

MNEMONIC	Pin Number							DESCRIPTION	
	LQFP64	LQFP48	LQFP44	PDIP40	SOP32	LQFP32	SOP28 SKDIP28		
P4.4/$\overline{RD}$ /PWM4_2	44	32	29	31	-	-	-	P4.4	common I/O port PORT4[4]
								$\overline{RD}$	Read pulse of external data memory
								PWM4_2	The fourth output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P4.5/ALE/ PWM3_2	57	41	38	40	-	-	-	P4.5	common I/O port PORT4[5]
								ALE	Address Latch Enable. It is used for external data memory cycles (MOVX)
								PWM3_2	The third output channel of Pulse Width Modulation. The port mode defauts to input-only(high-impedance) mode after power-on or reset
P4.6/ RxD2_2	58	42	39	-	-	-	-	P4.6	common I/O port PORT4[6]
								RxD2_2	Receive Data Port of UART2
P4.7/ TxD2_2	11	7	6	-	-	-	-	P4.7	common I/O port PORT4[7]
								TxD2_2	Transit Data Port of UART2
P5.0/ RxD3_2	32	24	-	-	-	-	-	P5.0	common I/O port PORT5[0]
								RxD3_2	Receive Data Port of UART3
P5.1/ TxD3_2	33	25	-	-	-	-	-	P5.1	common I/O port PORT5[1]
								TxD3_2	Transit Data Port of UART3
P5.2/ RxD4_2	64	48	-	-	-	-	-	P5.2	common I/O port PORT5[2]
								RxD4_2	Receive Data Port of UART4
P5.3/ TxD4_2	1	1	-	-	-	-	-	P5.3	common I/O port PORT5[3]
								TxD4_2	Transit Data Port of UART4
P5.4/RST/ MCLKO/ SS_3/CMP-	18	14	13	17	13	9	11	P5.4	common I/O port PORT5[4]
								RST	Reset pin. A high on this pin for at least two machine cycles will reset the device.
								MCLKO	Master clock output; the output frequency can be MCLK/1, MCLK/2 and MCLK/4. The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.
								SS_3	Slave selection signal of synchronous serial peripheral interface----SPI
								CMP-	Comparator negative input
P5.5/CMP+	20	16	15	19	15	11	13	P5.5	common I/O port PORT5[5]
								CMP+	Comparator positive input

MNEMONIC	Pin Number							DESCRIPTION
	LQFP64	LQFP48	LQFP44	PDIP40	SOP32	LQFP32	SOP28 SKDIP28	
P6.0	5							common I/O port PORT6[0]
P6.1	6							common I/O port PORT6[1]
P6.2	7							common I/O port PORT6[2]
P6.3	8							common I/O port PORT6[3]
P6.4	23							common I/O port PORT6[4]
P6.5	24							common I/O port PORT6[5]
P6.6	25							common I/O port PORT6[6]
P6.7	26							common I/O port PORT6[7]
P7.0	37							common I/O port PORT7[0]
P7.1	38							common I/O port PORT7[1]
P7.2	39							common I/O port PORT7[2]
P7.3	40							common I/O port PORT7[3]
P7.4	53							common I/O port PORT7[4]
P7.5	54							common I/O port PORT7[5]
P7.6	55							common I/O port PORT7[6]
P7.7	56							common I/O port PORT7[7]
Vcc	19	15	14	18	14	10	12	The positive pole of power
Gnd	21	17	16	20	16	12	14	The negative pole of power, Gound