# General Overview of STC15F2K60S2 series MCU

## 1 Introduction of STC15F2K60S2 series MCU (In abundant supply)

STC15F2K60S2 series MCU is a single-chip microcontroller based on a high performance 1T architecture 8051 CPU, which is produced by STC MCU Limited. It is a new generation of 8051 MCU of high speed, high stability, low power consumption and super strong anti-disturbance. Besides, STC15F2K60S2 series MCU is a MCU of super advanced encryption, because it adopts the eighth generation of STC encryption technology. With the enhanced kernel, STC15F2K60S2 series MCU is faster than a traditional 8051 in executing instructions (about 8~12 times the rate of a traditional 8051 MCU), and has a fully compatible instruction set with traditional 8051 series microcontroller. External expensive crystal can be removed by being integrated internal high-precise R/C clock(±0.3%) with ±1% temperature drift (-40℃~+85℃) while ±0.6% in normal temperature (-20℃~+65℃) and wide frenquency adjustable between 5MHz and 35MHz. External reset curcuit also can be removed by being integrated internal highly reliable one with 8 levels optional threshold voltage of reset. The STC15F2K60S2 series MCU retains all features of the traditional 8051. In addition, it has 3-channels CCP/PCA/PWM, 8-channels and 10-bits A/D Converter(300 thousand times per sec.), large capacity of 2K bytes SRAM, two high-speed asynchronous serial ports----UARTs(UART1/UART2, can be regarded as 5 serial ports by shifting among 5 groups of pins) and a high-speed synchronous serial peripheral interface----SPI. STC15F2K60S2 series MCU is usually used in communications which need for serveral UARTs or electrical control or some occasion with strong disturbance.

In Keil C development environment, select the Intel 8052 to compiling and only contain < reg51.h > as header file.

STC15 series MCU with super high-speed CPU core of STC-Y5 works 20% faster than STC early 1T series (such as STC12/STC11/STC10 series) at same clock frequency.

- Enhanced 8051 Central Processing Unit, 1T, single clock per machine cycle, faster 8~12 times than the rate of a traditional 8051.
- Operating voltage range:
  STC15F2K60S2 series: 5.5V ~ 4.2V (5V MCU).
  STC15L2K60S2 series: 3.6V ~ 2.4V (3V MCU).
- On-chip 8/16/24/32/40/48/56/60/61/63.5K FLASH program memory with flexible ISP/IAP capability, can be repeatedly erased more than 100 thousand times.
- Large capacity of on-chip 2048 bytes SRAM: 256 byte scratch-pad RAM and 1792 bytes of auxiliary RAM
- Be capable of addressing up to 64K byte of external RAM
- On-chip EEPROM with large capacity can be repeatedly erased more than 100 thousand times.
- Dual Data Pointer (DPTR) to speed up data movement
- ISP/IAP, In-System-Programming and In-Application-Programming , no need for programmer and emulator.
- 8 channels and 10 bits Analog-to-Digital Converter (ADC), the speed up to 300 thousand times per second, 3 channels PWM also can be used as 3 channels D/A Converter(DAC).
- 3 channels Capture/Compare uints(CCP/PCA/PWM)
  ---- can be used as 3 Times or 3 external Interrupts(can be generated on rising or falling edge) or 3 channels D/A Converter.

- The high-speed pulse function of CCP/PCA can be utilized to to realize 3 channels 9 ~ 16 bit PWM (each channel of which takes less than 0.6% system time)
- The clock output function of T0, T1 or T2 can be utilized to realize 8 ~ 16 bit PWM with a high degree of accuracy (which takes less than 0.4% system time)
- Internal hghly reliable Reset with 8 levels optional threshold voltage of reset, external reset curcuit can be completely removed
- Internal high- precise R/C clock(±0.3%) with ±1% temperature drift (-40℃~+85℃) while ±0.6% (-20℃ ~+65℃) in normal temperature and wide frenquency adjustable between 5MHz and 35MHz (5.5296MHz / 11.0592MHz / 22.1184MHz / 33.1776MHz).
- No need external crystal and reset, and can output clock and low reset signal from MCU.
- Operating frequency range: 0- 28MHz, is equivalent to traditional 8051:0~336MHz.
- Two high-speed asynchronous serial ports----UARTs (UART1/UART2 can be used simultaneously and regarded as 5 serial ports by shifting among 5 groups of pins):
  UART1(RxD/P3.0, TxD/P3.1) can be switched to (RxD_2/P3.6, TxD_2/P3.7),
  also can be switched to (RxD_3/P1.6, TxD_3/P1.7);
  UART2(RxD2/P1.0, TxD2/P1.1) can be switched to (RxD2_2/P4.6, TxD2_2/P4.7).
- A high-speed synchronous serial peripheral interface----SPI.
- Support the function of Encryption Download (to protect your code from being intercepted).
- Support the function of RS485 Control
- Code protection for flash memory access, excellent noise immunity, very low power consumption
- Power management mode: Slow-Down mode, Idle mode(all interrupt can wake up Idle mode), Stop/Power-Down mode.
- Timers which can wake up stop/power-down mode: have internal low-power special wake-up Timer.
- Resource which can wake up stop/power-down mode are: INT0/P3.2, INT1/P3.3 (INT0/INT1, may be generated on both rising and falling edges), $\overline{\text{INT2}}$/P3.6, $\overline{\text{INT3}}$/P3.7, $\overline{\text{INT4}}$/P3.0 ($\overline{\text{INT2}}$ /$\overline{\text{INT3}}$/$\overline{\text{INT4}}$, only be generated on falling edge); pins CCP0/CCP1/CCP2; pins T0/T1/T2(their falling edge can wake up if T0/T1/T2 have been enabled before power-down mode, but no interrupts can be generatetd); internal low-power special wake-up Timer.
- six Timers/Counters, threee 16-bit reloadable Timer/Counter(T0/T1/T2, T0 and T1 are compatible with Timer0/Timer1 of traditional 8051), T0/T1/T2 all can independently achieve external programmable clock output (3 channels), 3 channels CCP/PWM/PCA also can be used as three timers.
- Programmable clock output function(output by dividing the frequency of the internal system clock or the input clock of external pin):
  The speed of external programmable clock output of 5V MCU is also not more than 13.5MHz, because the output speed of I/O port of STC15 series 5V MCU is not more than 13.5MHz.
  The speed of external programmable clock output of 3.3V MCU is also not more than 8MHz, because the output speed of I/O port of STC15 series 3.3V MCU is not more than 8MHz.

① The Programmable clock output of T0 is on P3.5/T0CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T0/P3.4)
② The Programmable clock output of T1 is on P3.4/T1CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T1/P3.5)
③ The Programmable clock output of T2 is on P3.0/T2CLKO (output by dividing the frequency of the internal system clock or the input clock of external pin T2/P3.1)
Three timers/counters in above all can be output by dividing the frequency from 1 to 65536.
④ The Programmable clock output of master clock is on P5.4/MCLKO, and its frequency can be divided into MCLK/1, MCLK/2, MCLK/4.

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.

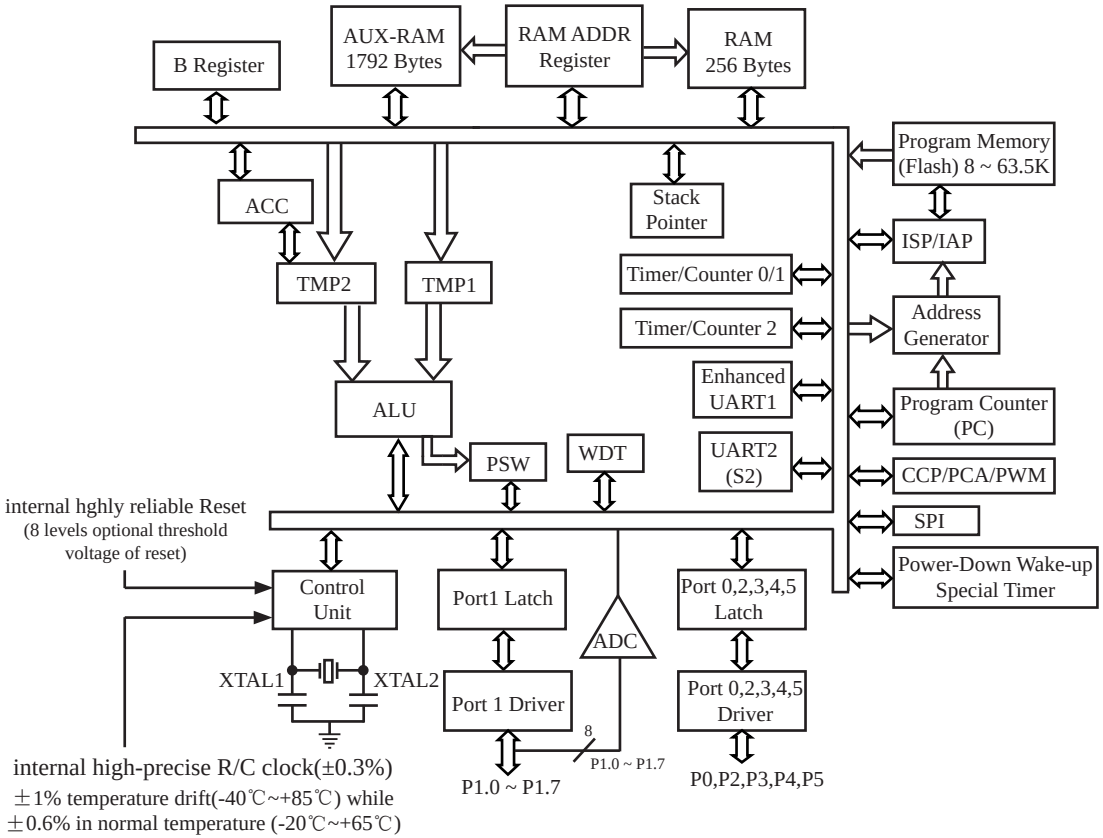
MCLK is the frequency of master clock. MCLKO is the output of master clock.

It is on MCLKO/P3.4 that the Programmable clock output of master clock of STC15 series 8-pin MCU (such as STC15F101W series). However, it is on MCLKO/P5.4 that the Programmable clock output of master clock of other STC15 series MCU including 16-pin or more than 16-pin MCU(such as STC15F2K60S2, STC15W4K32S4 and so on)

- One 15 bits Watch-Dog-Timer with 8-bit pre-scaler (one-time-enabled)
- advanced instruction set, which is fully compatible with traditional 8051 MCU, have hardware multiplication / division command.
- 42/38/30/26 common I/O ports are available, their mode is quasi_bidirectional/weak pull-up (traditional 8051 I/O ports mode) after reset, and can be set to four modes: quasi_bidirectional/weak pull-up, strong push-pull/ strong pull-up, input-only/high-impedance and open drain.
- the driving ability of each I/O port can be up to 20mA, but it don't exceed this maximum 120mA that the current of the whole chip of 40-pin or more than 40-pin MCU, while 90mA that the current of the whole chip of 16-pin or more than 16-pin MCU or 32-pin or less than 32-pin MCU.
- If I/O ports are not enough, it can be extended by connecting a 74HC595(reference price: RMB 0.15 yuan). Besides, cascading several chips also can extend to dozens of I/O ports.
- Package: LQFP44 (12mm x 12mm), LQFP-32 (9mm x 9mm), TSSOP20(6.5mm x 6.5mm), SOP28, SKDIP28, PDIP-40.
- All products are baked 8 hours in high-temperature 175℃ after be packaged, Manufacture guarantee good quality.
- In Keil C development environment, select the Intel 8052 to compiling and only contain < reg51.h > as header file.

# 2 Block diagram of STC15F2K60S2 series

The internal structure of STC15F2K60S2 series MCU is shown in the block diagram below. STC15F2K60S2 series MCU includes central processor unit(CPU), program memory (Flash), data memory(SRAM), Timers/ Counters, I/O ports, high-speed A/D converter(ADC), watchdog, high-speed asynchronous serial communication ports---UART(UART1/UART2), CCP/PWM/PCA, a group of high-speed synchronous serial peripheral interface (SPI), internal high- precise R/C clock, internal hghly reliable Reset and so on. STC15F2K60S2 series MCU almost includes all of the modules required in data acquisition and control, and can be regarded as an on-chip system (SysTem Chip or SysTem on Chip, abbreviated as STC, this is the name origin of Hongjing technology STC Limited).




STC15F2K60S2 series Block Diagram

# 3 Pin Configurations of STC15F2K60S2 series MCU

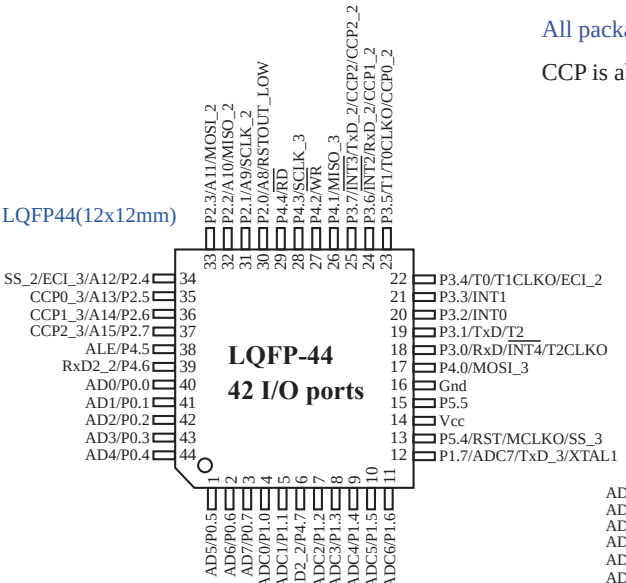
All packages meet EU RoHS standards

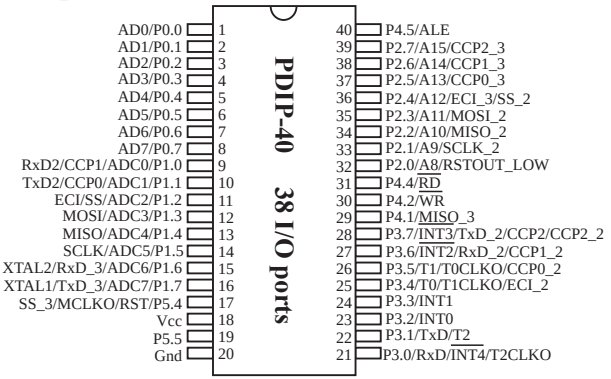
CCP is abbreviation for Capture, Compare, PWM

Note：P0 ports can be multiplexed as Address/Data bus，not as A/D Converter. 8 channels of A/D Converter are on P1.

Consequently：P0.x/ADx means that P0.x can be used as Address/Data bus, while P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.

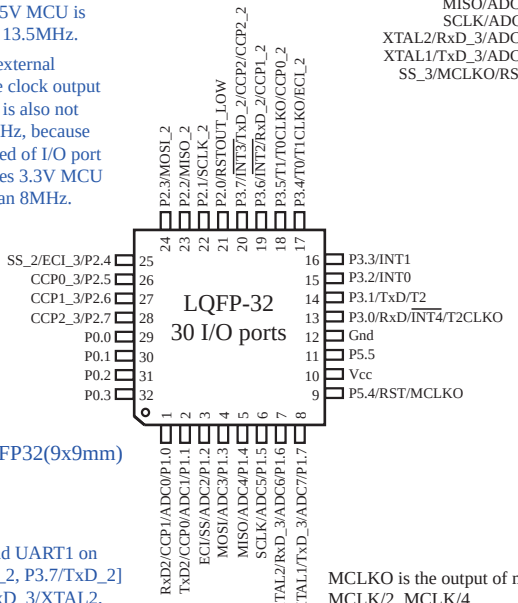
LQFP44(12x12mm)




The speed of external programmable clock output of 5V MCU is also not more than 13.5MHz, because the output speed of I/O port of STC15 series 5V MCU is not more than 13.5MHz.

The speed of external programmable clock output of 3.3V MCU is also not more than 8MHz, because the output speed of I/O port of STC15 series 3.3V MCU is not more than 8MHz.




LQFP32(9x9mm)

Recommend UART1 on [P3.6/RxD_2, P3.7/TxD_2] or [P1.6/RxD_3/XTAL2, P1.7/TxD_3/XTAL1]

T0CLKO refers to the programmable clock output of Timer/Counter 0
(output by dividing the frequency of the internal system clock or the input clock of external pin T0/P3.4);

T1CLKO refers to the programmable clock output of Timer/Counter 1
(output by dividing the frequency of the internal system clock or the input clock of external pin T1/P3.5);

T2CLKO refers to the programmable clock output of Timer/Counter 2
(output by dividing the frequency of the internal system clock or the input clock of external pin T2/P3.1);

In addition to programmable output on the internal system clock, T0CLKO/T1CLKO/T2CLKO also can be used as divider by dividing the frequency of the internal system clock or the input clock of external pin T0/T1/T2.

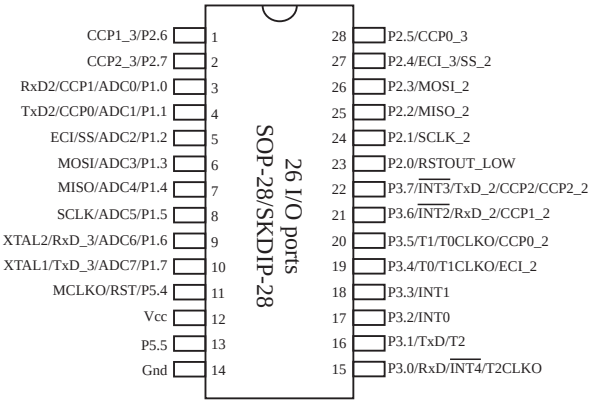
MCLKO is the output of master clock whose frequency can be divided into MCLK/1, MCLK/2, MCLK/4
The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator. MCLK is the frequency of master clock.

CCP is abbreviation for Capture, Compare, PWM

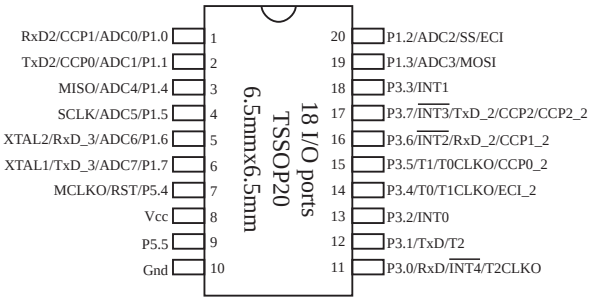
8 channels of A/D Converter are on P1. P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.

The speed of external programmable clock output of 5V MCU is also not more than 13.5MHz, because the output speed of I/O port of STC15 series 5V MCU is not more than 13.5MHz.

The speed of external programmable clock output of 3.3V MCU is also not more than 8MHz, because the output speed of I/O port of STC15 series 3.3V MCU is not more than 8MHz.




Recommend UART1 on [P3.6/RxD_2, P3.7/TxD_2] or [P1.6/RxD_3/XTAL2, P1.7/TxD_3/XTAL1]




MCLKO is the output of master clock whose frequency can be divided into MCLK/**1, MCLK/2, MCLK/4**
The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator. MCLK is the frequency of master clock.

T0CLKO refers to the programmable clock output of Timer/Counter 0
(output by dividing the frequency of the internal system clock or the input clock of external pin T0/P3.4);

T1CLKO refers to the programmable clock output of Timer/Counter 1
(output by dividing the frequency of the internal system clock or the input clock of external pin T1/P3.5);

T2CLKO refers to the programmable clock output of Timer/Counter 2
(output by dividing the frequency of the internal system clock or the input clock of external pin T2/P3.1);

In addition to programmable output on the internal system clock, T0CLKO/T1CLKO/T2CLKO also can be used as divider by dividing the frequency of the internal system clock or the input clock of external pin T0/T1/T2.

| Mnemonic | Add | Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AUXR1 P_SW1 | A2H | Auxiliary register 1 | S1_S1 | S1_S0 | CCP_S1 | CCP_S0 | SPI_S1 | SPI_S0 | 0 | DPS | 0100,0000 |
| P_SW2 | BAH | Peripheral function switch register | | | | | | S4_S | S3_S | S2_S | xxxx,xxx0 |
| CLK_DIV (PCON2) | 97H | Clock Division register | MCKO_S1 | MCKO_S0 | ADRJ | Tx_Rx | Tx2_Rx2 | CLKS2 | CLKS1 | CLKS0 | 0000,x000 |

| UART1/S1 can be switched in 3 groups of pins by selecting the control bits S1_S0 and S1_S1. | | |
|---|---|---|
| S1_S1 | S1_S0 | UART1/S1 can be switched between P1 and P3 |
| 0 | 0 | UART1/S1 on [P3.0/RxD,P3.1/TxD] |
| 0 | 1 | UART1/S1 on [P3.6/RxD_2,P3.7/TxD_2] |
| 1 | 0 | UART1/S1 on [P1.6/RxD_3/XTAL2,P1.7/TxD_3/XTAL1] when UART1 is on P1, please using internal R/C clock. |
| 1 | 1 | Invalid |

Recommed UART1 on [P3.6/RxD_2,P3.7/TxD_2] or [P1.6/RxD_3/XTAL2,P1.7/TxD_3/XTAL1].

| CCP can be switched in 3 groups of pins by selecting the control bits CCP_S1 and CCP_S0. | | |
|---|---|---|
| CCP_S1 | CCP_S0 | CCP can be switched in P1 and P2 and P3 |
| 0 | 0 | CCP on [P1.2/ECI,P1.1/CCP0,P1.0/CCP1,P3.7/CCP2] |
| 0 | 1 | CCP on [P3.4/ECI_2,P3.5/CCP0_2,P3.6/CCP1_2,P3.7/CCP2_2] |
| 1 | 0 | CCP on [P2.4/ECI_3,P2.5/CCP0_3,P2.6/CCP1_3,P2.7/CCP2_3] |
| 1 | 1 | Invalid |

| SPI can be switched in 3 groups of pins by selecting the control bits SPI_S1 and SPI_S0 | | |
|---|---|---|
| SPI_S1 | SPI_S0 | SPI can be switched in P1 and P2 and P4 |
| 0 | 0 | SPI on [P1.2/SS,P1.3/MOSI,P1.4/MISO,P1.5/SCLK] |
| 0 | 1 | SPI on [P2.4/SS_2,P2.3/MOSI_2,P2.2/MISO_2,P2.1/SCLK_2] |
| 1 | 0 | SPI on [P5.4/SS_3,P4.0/MOSI_3,P4.1/MISO_3,P4.3/SCLK_3] |
| 1 | 1 | Invalid |

| UART2/S2 can be switched in 2 groups of pins by selecting the control bit S2_S. | |
|---|---|
| S2_S | UART2/S2 can be switched between P1 and P4 |
| 0 | UART2/S2 on [P1.0/RxD2,P1.1/TxD2] |
| 1 | UART2/S2 on [P4.6/RxD2_2,P4.7/TxD2_2] |

DPS：DPTR registers select bit.

0: DPTR0 is selected

1: DPTR1 is selected

| Mnemonic | Add | Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CLK_DIV (PCON2) | 97H | Clock Division register | MCKO_S1 | MCKO_S0 | ADRJ | Tx_Rx | Tx2_Rx2 | CLKS2 | CLKS1 | CLKS0 | 0000,x000 |

| MCKO_S1 | MCKO_S0 | the control bit of master clock output by dividing the frequency (The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator) |
|---|---|---|
| 0 | 0 | Master clock do not output external clock |
| 0 | 1 | Master clock output external clock，but its frequency do not be divided，and the output clock frequency = MCLK / 1 |
| 1 | 0 | Master clock output external clock，but its frequency is divided by 2，and the output clock frequency = MCLK / 2 |
| 1 | 1 | Master clock output external clock，but its frequency is divided by 4，and the output clock frequency = MCLK / 4 |

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator. MCLK is the frequency of master clock.

STC15F2K60S2 series MCU output master clock on MCLKO/P5.4

It is on MCLKO/P3.4 that the Programmable clock output of master clock of STC15 series 8-pin MCU (such as STC15F101W series). However, it is on MCLKO/P5.4 that the Programmable clock output of master clock of other STC15 series MCU including 16-pin or more than 16-pin MCU.

ADRJ：the adjustment bit of ADC result

0：ADC_RES[7:0] store high 8-bit ADC result，ADC_RESL[1:0] store low 2-bit ADC result

1：ADC_RES[1:0] store high 2-bit ADC result，ADC_RESL[7:0] store low 8-bit ADC result

Tx_Rx：the set bit of relay and broadcast mode of UART1

0：UART1 works on normal mode

1：UART1 works on relay and broadcast mode，that to say output the input level state of RxD port to the outside TxD pin in real time, namely the external output of TxD pin can reflect the input level state of RxD port.

the RxD and TxD of UART1 can be switched in 3 groups of pins: [RxD/P3.0, TxD/P3.1];
[RxD_2/P3.6, TxD_2/P3.7];
[RxD_3/P1.6, TxD_3/P1.7].

Tx2_Rx2：the set bit of relay and broadcast mode of UART2，the function is reserved temporarily.
the RxD2 and TxD2 of UART2 can be switched in 2 groups of pins: [RxD2/P1.0, TxD2/P1.1];
[RxD2_2/P4.6, TxD2_2/P4.7].

| CLKS2 | CLKS1 | CLKS0 | the control bit of system clock (System clock refers to the master clock that has been divided frequency, which is offered to CPU, UARTs, SPI, Timers, CCP/PWM/PCA and A/D Converter) |
|---|---|---|---|
| 0 | 0 | 0 | Master clock frequency/1, No division |
| 0 | 0 | 1 | Master clock frequency/2 |
| 0 | 1 | 0 | Master clock frequency/4 |
| 0 | 1 | 1 | Master clock frequency/8 |
| 1 | 0 | 0 | Master clock frequency/16 |
| 1 | 0 | 1 | Master clock frequency/32 |
| 1 | 1 | 0 | Master clock frequency/64 |
| 1 | 1 | 1 | Master clock frequency/128 |

The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator.

# 4 STC15F2K60S2 series Selection and Price Table

| Type 1T 8051 MCU | Operating Voltage (V) | Flash (byte) | SRAM (byte) | UART | SPI | common Timers T0-T2 | CCP PCA PWM | Speical Power-down Wake-up Timer | Standard External Interrupts | A/D 8-channel | DPTR | EEPROM | Internal Low-Voltage Detection Interrupt | WDT | Internal High-reliable Reset (with optional threshold voltage) | Internal High-Precise Clock | Output clock and reset signal from MCU | Encryption Download (to protect your code from being intercepted) | RS485 Control | All Packages LQFP44 PDIP40 LQFP32 SOP28 SKDIP28 TSSOP20 Price of a part of packages(RMB ¥) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | LQFP44 | SOP28 |
| STC15F2K60S2 series MCU Selection and Price Table<br>Note: 3 channels CCP/PCA/PWM also can be used as 3 Timers. | | | | | | | | | | | | | | | | | | | | | |
| STC15F2K08S2 | 5.5-4.2 | 8K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 53K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15F2K16S2 | 5.5-4.2 | 16K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 45K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15F2K24S2 | 5.5-4.2 | 24K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 37K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15F2K32S2 | 5.5-4.2 | 32K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 29K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15F2K40S2 | 5.5-4.2 | 40K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 22K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15F2K48S2 | 5.5-4.2 | 48K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 13K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15F2K56S2 | 5.5-4.2 | 56K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 5K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15F2K60S2 | 5.5-4.2 | 60K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 1K | Y | Y | 8-level | Y | Y | Y | Y | | |
| IAP15F2K61S2 (which itself is a emluator) | 5.5-4.2 | 61K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | IAP | Y | Y | 8-level | Y | Y | Y | Y | | The program Flash in user program area can be used as EEPROM. |
| IRC15F2K63S2 (Using external crystal or internal 24MHz clock) | 5.5-4.2 | 63.5K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | IAP | Y | Y | Fixed | Y | Y | N | N | | - The program Flash in user program area can be used as EEPROM. |
| IAP15F2K61S | 5.5-4.2 | 61K | 2K | 1 | Y | 3 | N | Y | 5 | N | 2 | IAP | Y | Y | 8-level | Y | Y | Y | Y | | - The program Flash in user program area can be used as EEPROM. |
| STC15F2K24AS | 5.5-4.2 | 24K | 2K | 1 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 5K | Y | Y | 8-level | Y | Y | Y | Y | | - |
| STC15L2K60S2 series MCU Selection and Price Table | | | | | | | | | | | | | | | | | | | | | |
| STC15L2K08S2 | 2.4-3.6 | 8K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 53K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15L2K16S2 | 2.4-3.6 | 16K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 45K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15L2K24S2 | 2.4-3.6 | 24K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 37K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15L2K32S2 | 2.4-3.6 | 32K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 29K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15L2K40S2 | 2.4-3.6 | 40K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 22K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15L2K48S2 | 2.4-3.6 | 48K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 13K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15L2K56S2 | 2.4-3.6 | 56K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 5K | Y | Y | 8-level | Y | Y | Y | Y | | |
| STC15L2K60S2 | 2.4-3.6 | 60K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | 1K | Y | Y | 8-level | Y | Y | Y | Y | | |
| IAP15L2K61S2 (which itself is a emluator) | 2.4-3.6 | 61K | 2K | 2 | Y | 3 | 3-ch | Y | 5 | 10-bit | 2 | IAP | Y | Y | 8-level | Y | Y | Y | Y | | The program Flash in user program area can be used as EEPROM. |
| IAP15L2K61S | 2.4-3.6 | 61K | 2K | 1 | Y | 3 | N | Y | 5 | N | 2 | IAP | Y | Y | 8-level | Y | Y | Y | Y | | - The program Flash in user program area can be used as EEPROM. |

Encryption Download : please burn source code with encryption key onto MCU in the factory. Then, you can make a simple update software just with one "update" button by fisrtly using the fuction "encrytion download" and then "release project" to update yourself code unabled to be intercepted when you need to upgrade your code.

To provide customized IC services

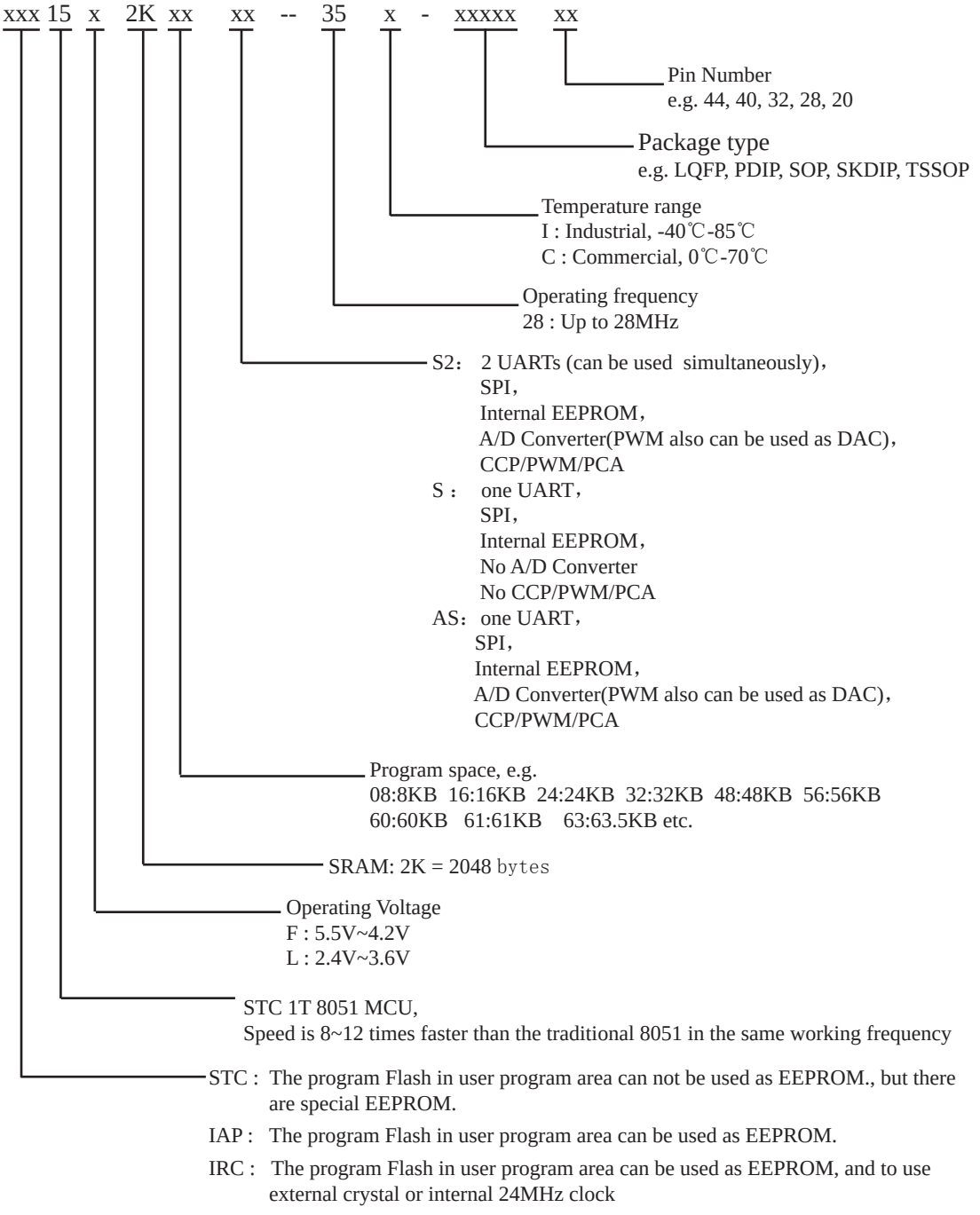
Because the last 7 bytes of the program area is stored mandatorily the contents of only global ID, the program space the user can actually use is 7 bytes smaller than the space shown in the selection table.

Conclusion: STC15F2K60S2 series MCU have: Three 16-bit relaodable Timers/Counters that are Timer/Counter 0, Timer/Counter 1 and Timer/Counter 2; 3 channels CCP/PWM/PCA (can achieve 3 timers or 3 D/A converters again); special power-down wake-up timer; 5 external interrupts INT0/INT1/$\overline{\text{INT2}}$/$\overline{\text{INT3}}$/$\overline{\text{INT4}}$; 2 high-speed asynchronous serial ports ---- UARTs (UART1/UART2 can be used simultaneously); a high-speed synchronous serial peripheral interface ---- SPI; 8 channels and 10 bits high-speed A/D converter; 2 data pointers ---- DPTR; external data bus and so on.

# 5 STC15F2K60S2 series Package and Price Table

| Type 1T 8051 MCU | Operating Voltage (V) | Operating Frequency (MHz) | Operating Temprature (I — Industrial) | All Packages Price( RMB ¥) LQFP44 / PDIP40 LQFP32 SOP28 / SKDIP28 TSSOP20 | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | LQFP44 | PDIP40 | LQFP32 | SOP28 | SKDIP28 | TSSOP20 |
| STC15F2K60S2 series MCU Package and Price Table | | | | | | | | | |
| STC15F2K08S2 | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | | | | - |
| STC15F2K16S2 | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | | | | - |
| STC15F2K24S2 | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | | | | - |
| STC15F2K32S2 | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | | | | - |
| STC15F2K40S2 | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | | | | - |
| STC15F2K48S2 | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | | | | - |
| STC15F2K56S2 | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | | | | - |
| STC15F2K60S2 | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | | | | - |
| IAP15F2K61S2 (which itself is a emluator) | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | | | | |
| IRC15F2K63S2 (Using external crystal or internal 24MHz clock) | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | - | - | - | - |
| IAP15F2K61S | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | | - | - | - | - |
| STC15F2K24AS | 5.5-4.2 | 28 | -40℃ ~ +85℃ | | - | - | - | - | - |
| STC15L2K60S2 series MCU Package and Price Table | | | | | | | | | |
| STC15L2K08S2 | 2.4-3.6 | 28 | -40℃ ~ +85℃ | | - | | | - | - |
| STC15L2K16S2 | 2.4-3.6 | 28 | -40℃ ~ +85℃ | | - | | | - | - |
| STC15L2K24S2 | 2.4-3.6 | 28 | -40℃ ~ +85℃ | | - | | | - | - |
| STC15L2K32S2 | 2.4-3.6 | 28 | -40℃ ~ +85℃ | | - | | | - | - |
| STC15L2K40S2 | 2.4-3.6 | 28 | -40℃ ~ +85℃ | | - | | | - | - |
| STC15L2K48S2 | 2.4-3.6 | 28 | -40℃ ~ +85℃ | | - | | | - | - |
| STC15L2K56S2 | 2.4-3.6 | 28 | -40℃ ~ +85℃ | | - | | | - | - |
| STC15L2K60S2 | 2.4-3.6 | 28 | -40℃ ~ +85℃ | | - | | | - | - |
| IAP15L2K61S2 (which itself is a emluator) | 2.4-3.6 | 28 | -40℃ ~ +85℃ | | | | | | - |
| IAP15L2K61S | 2.4-3.6 | 28 | -40℃ ~ +85℃ | | - | - | - | - | - |

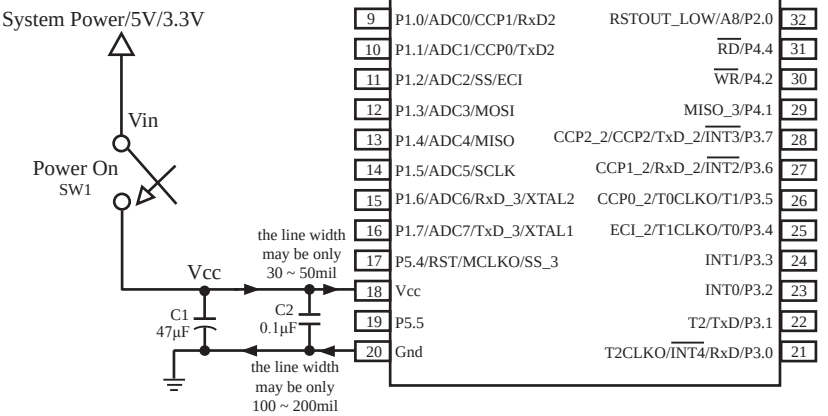
# 6 Naming rules of STC15F2K60S2 series MCU



# 7 Minimum Application System of STC15F2K60S2 Series MCU

Note：P0 ports can be multiplexed as Address/Data bus，not as A/D Converter. 8 channels of A/D Converter are on P1.

Consequently：P0.x/ADx means that P0.x can be used as Address/Data bus, while P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.




Internal hghly reliable Reset, External reset circuit can be completely removed.

P5.4/RST/MCLKO pin factory defaults to the I/O port, which can be set as RST reset pin(active high) through the STC-ISP programmer.

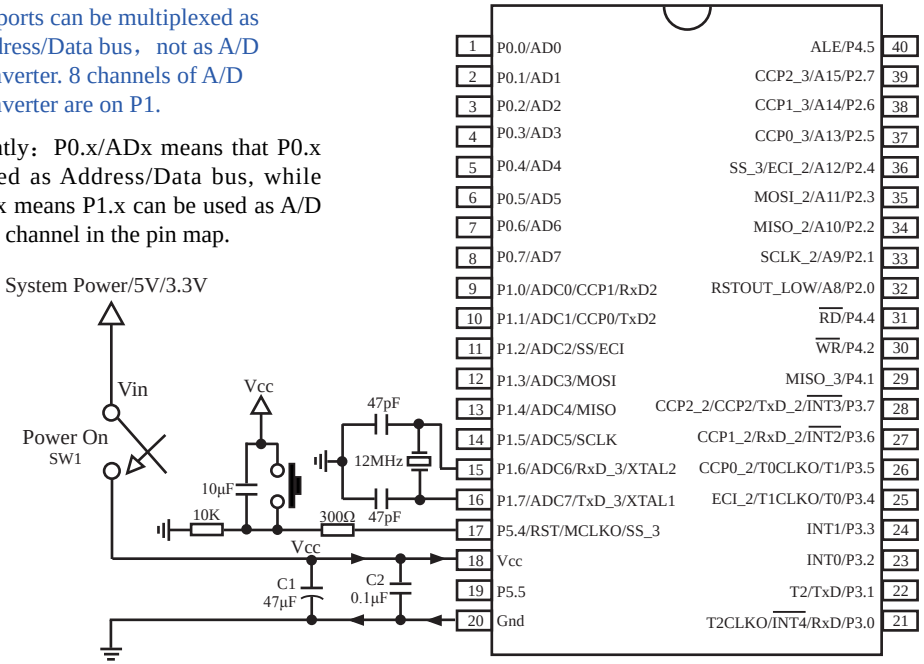
Internal high-precise R/C clock( ±3% ), ±1% temperature drift (-40℃~+85℃) while ±0.6% in normal temperature (-20℃~+65℃). External expensive crysal can be completely removed.

Recommend to add decoupling capacitor C1(47μF) and C2(0.1μF) between Vcc and Gnd that can remove power noise and improve the anti-interference ability.

# 8 Circuit Diagram connecting External Crystal Oscillator and Reset

Note：P0 ports can be multiplexed as Address/Data bus，not as A/D Converter. 8 channels of A/D Converter are on P1.

Consequently：P0.x/ADx means that P0.x can be used as Address/Data bus, while P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.




Internal hghly reliable Reset. External reset circuit can be completely removed, which also can be used as shown in above diagram.

P5.4/RST/MCLKO pin factory defaults to the I/O port, which can be set as RST reset pin(active high) through the STC-ISP programmer.

Internal high-precise R/C clock( ±3% ), ±1% temperature drift (-40℃~+85℃) while ±0.6% in normal temperature (-20℃~+65℃) . External expensive crysal can be completely removed, which also can be used as shown in above diagram. MCU defaults to use internal high precise R/C clock. Please select the option "external crystal or clock" when programming the STC-ISP programmer, if users require the use of external crystal oscillator.

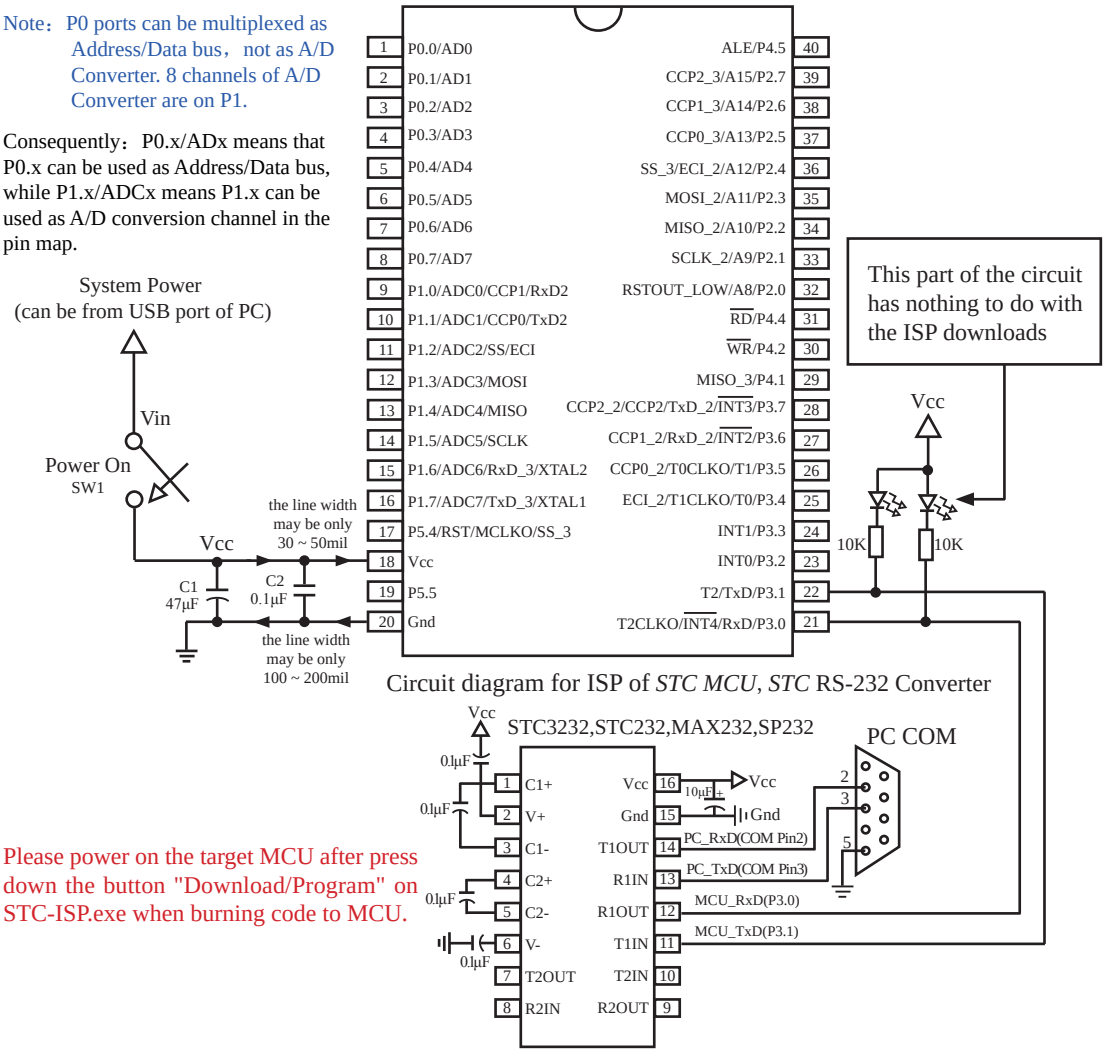
Recommend to add decoupling capacitor C1(47μF) and C2(0.1μF) between Vcc and Gnd that can remove power noise and improve the anti-interference ability.

# 9 Application Circuit Diagram for ISP of STC15F2K60S2 series MCU

## 9.1 Application Circuit Diagram for ISP using RS-232 Converter

Note：P0 ports can be multiplexed as Address/Data bus，not as A/D Converter. 8 channels of A/D Converter are on P1.

Consequently：P0.x/ADx means that P0.x can be used as Address/Data bus, while P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.




Please power on the target MCU after press down the button "Download/Program" on STC-ISP.exe when burning code to MCU.

Internal hghly reliable Reset. External reset circuit can be completely removed, which also can be used .

P5.4/RST/MCLKO pin factory defaults to the I/O port, which can be set as RST reset pin(active high) through the STC-ISP programmer.

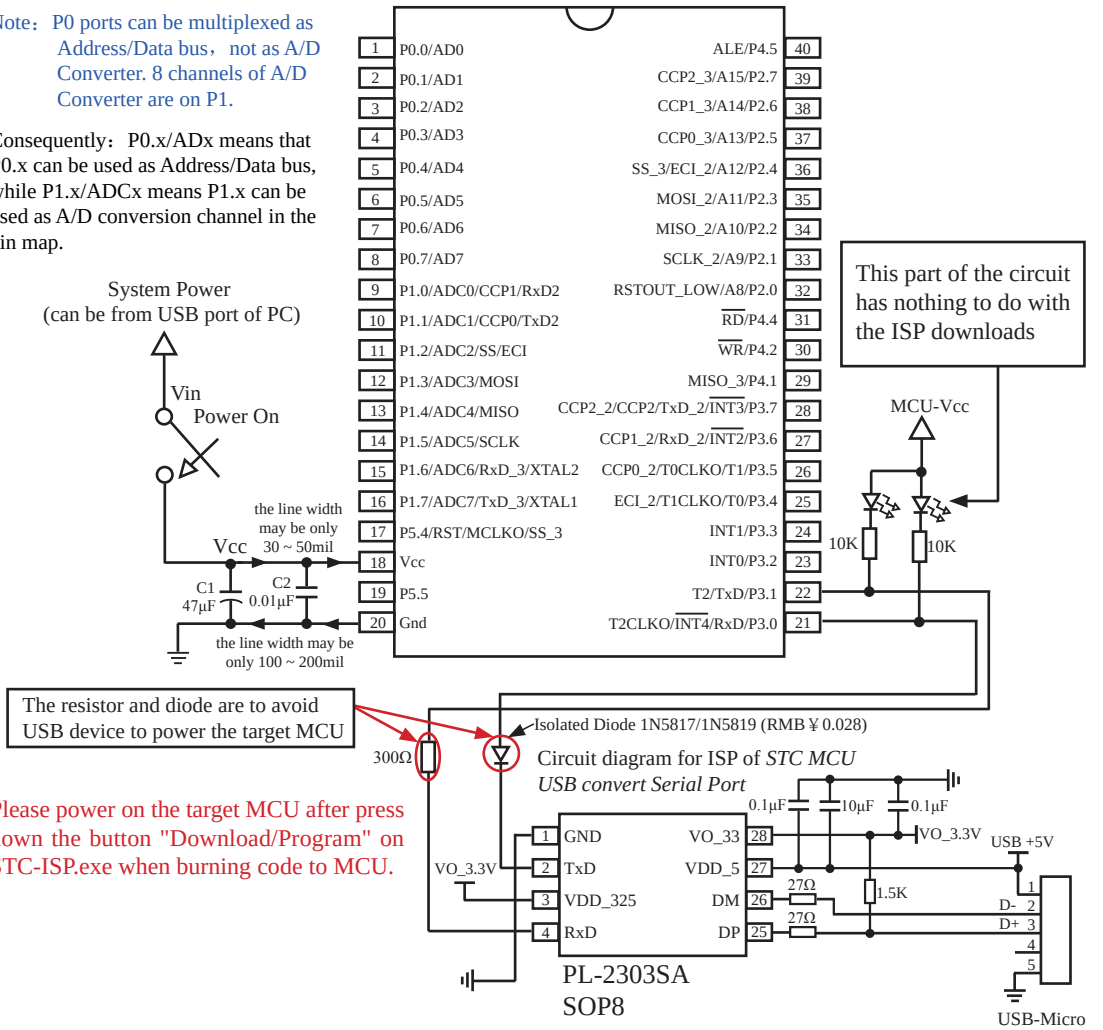
Internal high-precise R/C clock( ±3% ), ±1% temperature drift (-40℃~+85℃) while ±0.6% in normal temperature (-20℃~+65℃) . External expensive crysal can be completely removed, which also can be used.

Recommend to add decoupling capacitor C1(47μF) and C2(0.1μF) between Vcc and Gnd that can remove power noise and improve the anti-interference ability.

## 9.2 Application Circuit Diagram for ISP using USB Chip PL-2303SA to convert Serial Port

Note：P0 ports can be multiplexed as Address/Data bus，not as A/D Converter. 8 channels of A/D Converter are on P1.

Consequently：P0.x/ADx means that P0.x can be used as Address/Data bus, while P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.




Please power on the target MCU after press down the button "Download/Program" on STC-ISP.exe when burning code to MCU.

Internal hghly reliable Reset. External reset circuit can be completely removed, which also can be used .

P5.4/RST/MCLKO pin factory defaults to the I/O port, which can be set as RST reset pin(active high) through the STC-ISP programmer.

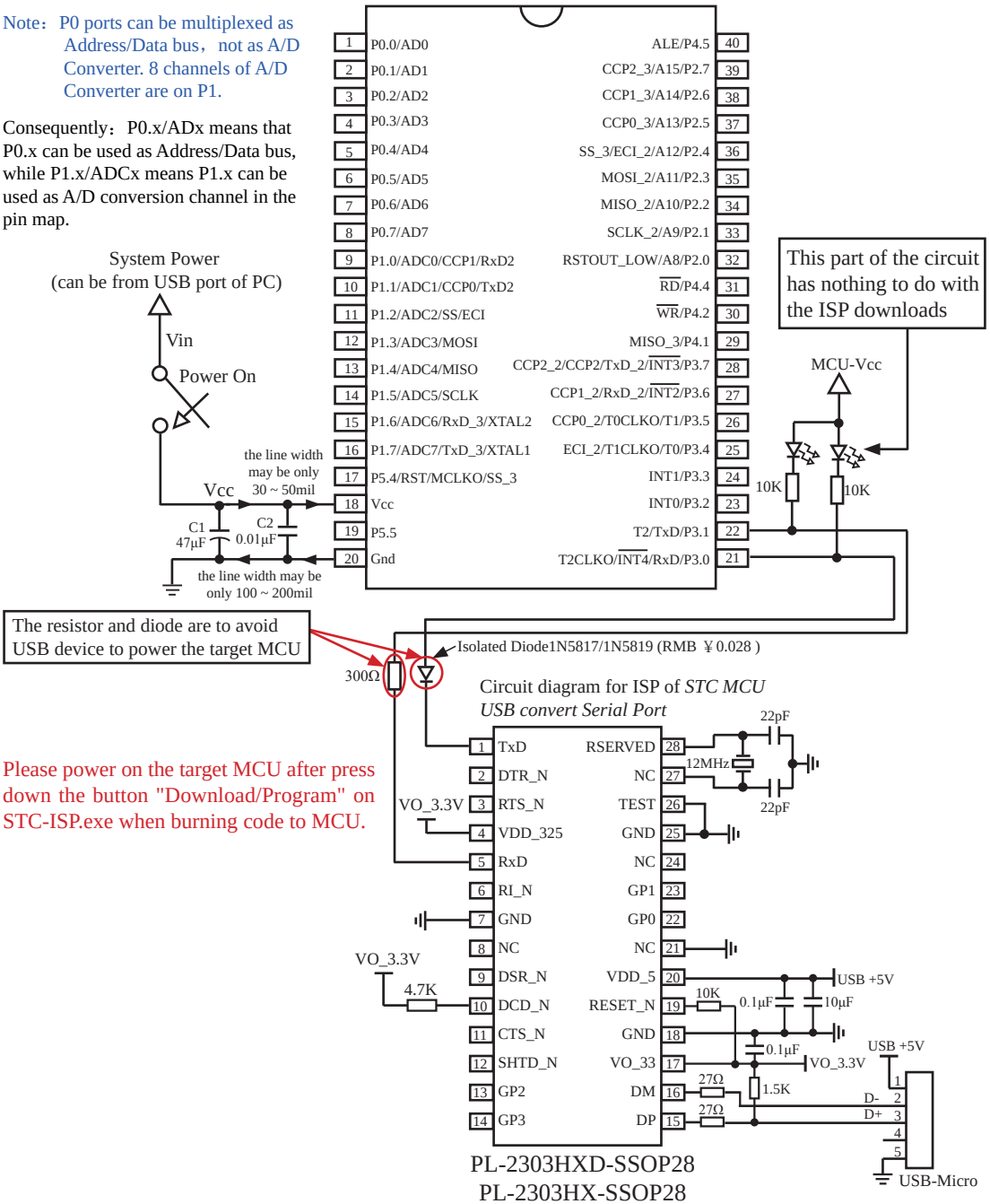
Internal high-precise R/C clock( ±3% ), ±1% temperature drift (-40℃~+85℃) while ±0.6% in normal temperature (-20℃~+65℃) . External expensive crysal can be completely removed, which also can be used.

Recommend to add decoupling capacitor C1(47μF) and C2(0.1μF) between Vcc and Gnd that can remove power noise and improve the anti-interference ability.

## 9.3 Application Circuit Diagram for ISP using USB Chip PL-2303HXD / PL-2303HX to convert Serial Port

Note：P0 ports can be multiplexed as Address/Data bus，not as A/D Converter. 8 channels of A/D Converter are on P1.

Consequently：P0.x/ADx means that P0.x can be used as Address/Data bus, while P1.x/ADCx means P1.x can be used as A/D conversion channel in the pin map.



# 10 Pin Descriptions of STC15F2K60S2 series MCU

| MNEMONIC | Pin Number | | | | | | | DESCRIPTION | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP44 | PLCC44 | PDIP40 | SOP32 | LQFP32 | SOP28 SKDIP28 | TSSOP20 | | |
| P0.0/AD0 | 40 | 2 | 1 | 1 | 29 | - | | P0.0 | common I/O port PORT0[0] |
| P0.1/AD1 | 41 | 3 | 2 | 2 | 30 | - | | P0.1 | common I/O port PORT0[1] |
| P0.2/AD2 | 42 | 4 | 3 | 3 | 31 | - | | P0.2 | common I/O port PORT0[2] |
| P0.3/AD3 | 43 | 5 | 4 | 4 | 32 | - | | P0.3 | common I/O port PORT0[3] |
| P0.4/AD4 | 44 | 6 | 5 | - | - | - | | P0.4 | common I/O port PORT0[4] |
| P0.5/AD5 | 1 | 7 | 6 | - | - | - | | P0.5 | common I/O port PORT0[5] |
| P0.6/AD5 | 2 | 8 | 7 | - | - | - | | common I/O port PORT0[6] | |
| P0.7/AD7 | 3 | 9 | 8 | - | - | - | | common I/O port PORT0[7] | |
| P1.0/ADC0/ CCP1/RxD2 | 4 | 10 | 9 | 5 | 1 | 3 | 1 | P1.0 | common I/O port PORT1[0] |
| | | | | | | | | ADC0 | ADC input channel-0 |
| | | | | | | | | CCP1 | Capture of external signal(measure frequency or be used as external interrupts)、high-speed Pulse and Pulse-Width Modulation output channel-1 |
| | | | | | | | | RxD2 | Receive Data Port of UART2 |
| P1.1/ADC1/ CCP0/TxD2 | 5 | 11 | 10 | 6 | 2 | 4 | 2 | P1.1 | common I/O port PORT1[1] |
| | | | | | | | | ADC1 | ADC input channel-1 |
| | | | | | | | | CCP0 | Capture of external signal(measure frequency or be used as external interrupts)、high-speed Pulse and Pulse-Width Modulation output channel-0 |
| | | | | | | | | TxD2 | Transit Data Port of UART2 |
| P1.2/ADC2/SS/ ECI | 7 | 13 | 11 | 7 | 3 | 5 | 20 | P1.2 | common I/O port PORT1[2] |
| | | | | | | | | ADC2 | ADC input channel-2 |
| | | | | | | | | SS | Slave selection signal of synchronous serial peripheral interface----SPI |
| | | | | | | | | ECI | External pulse input pin of CCP/PCA counter |
| P1.3/ADC3/ MOSI | 8 | 14 | 12 | 8 | 4 | 6 | 19 | P1.3 | common I/O port PORT1[3] |
| | | | | | | | | ADC3 | ADC input channel-3 |
| | | | | | | | | MOSI | Master Output Slave Input of SPI |
| P1.4/ADC4/ MISO | 9 | 15 | 13 | 9 | 5 | 7 | 3 | P1.4 | common I/O port PORT1[4] |
| | | | | | | | | ADC4 | ADC input channel-4 |
| | | | | | | | | MISO | Master Iutput Slave Onput of SPI |
| P1.5/ADC5/ SCLK | 10 | 16 | 14 | 10 | 6 | 8 | 4 | P1.5 | common I/O port PORT1[5] |
| | | | | | | | | ADC5 | ADC input channel-5 |
| | | | | | | | | SCLK | Clock Signal of synchronous serial peripheral interface----SPI |

| MNEMONIC | Pin Number | | | | | | | DESCRIPTION | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP44 | PLCC44 | PDIP40 | SOP32 | LQFP32 | SOP28 SKDIP28 | TSSOP20 | | |
| P1.6/ADC6/ RxD_3/XTAL2 | 11 | 17 | 15 | 11 | 7 | 9 | 5 | P1.6 | common I/O port PORT1[6] |
| | | | | | | | | ADC6 | ADC input channel--6 |
| | | | | | | | | RxD_3 | Receive Data Port of UART1 |
| | | | | | | | | XTAL2 | Output from the inverting amplifier of internal clock circuit. This pin should be floated when an external oscillator is used. |
| P1.7/ADC7/ TxD_3/XTAL1 | 12 | 18 | 16 | 12 | 8 | 10 | 6 | P1.7 | common I/O port PORT1[7] |
| | | | | | | | | ADC7 | ADC input channel--7 |
| | | | | | | | | TxD_3 | Transit Data Port of UART1 |
| | | | | | | | | XTAL1 | Input to the inverting oscillator amplifier of internal clock circuit. Receives the external oscillator signal when an external oscillator is used. |
| P2.0/ RSTOUT_LOW | 30 | 36 | 32 | 25 | 21 | 23 | | P2.0 | common I/O port PORT2[0] |
| | | | | | | | | RSTOUT_LOW | the pin output low after power-on and during reset, which can be set to output high by software |
| P2.1/SCLK_2 | 31 | 37 | 33 | 26 | 22 | 24 | | P2.1 | common I/O port PORT2[1] |
| | | | | | | | | SCLK_2 | Clock Signal of synchronous serial peripheral interface----SPI |
| P2.2/MISO_2 | 32 | 38 | 34 | 27 | 23 | 25 | | P2.2 | common I/O port PORT2[2] |
| | | | | | | | | MISO_2 | Master Iutput Slave Onput of SPI |
| P2.3/MOSI_2 | 33 | 39 | 35 | 28 | 24 | 26 | | P2.3 | common I/O port PORT2[3] |
| | | | | | | | | MOSI_2 | Master Output Slave Input of SPI |
| P2.4/ECI_3/ SS_2 | 34 | 40 | 36 | 29 | 25 | 27 | | P2.4 | common I/O port PORT2[4] |
| | | | | | | | | ECI_3 | External pulse input pin of CCP/ PCA counter |
| | | | | | | | | SS_2 | Slave selection signal of synchronous serial peripheral interface----SPI |
| P2.5/CCP0_3 | 35 | 41 | 37 | 30 | 26 | 28 | | P2.5 | common I/O port PORT2[5] |
| | | | | | | | | CCP0_3 | Capture of external signal(measure frequency or be used as external interrupts)、high-speed Pulse and Pulse-Width Modulation output channel-0 |
| P2.6/CCP1_3 | | 42 | 38 | 31 | 27 | 1 | | P2.6 | common I/O port PORT2[6] |
| | | | | | | | | CCP1_3 | Capture of external signal(measure frequency or be used as external interrupts)、high-speed Pulse and Pulse-Width Modulation output channel-1 |

| MNEMONIC | Pin Number | | | | | | | DESCRIPTION | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP44 | PLCC44 | PDIP40 | SOP32 | LQFP32 | SOP28 SKDIP28 | TSSOP20 | | |
| P2.7/CCP2_3 | 37 | 43 | 39 | 32 | 28 | 2 | | P2.7 | common I/O port PORT2[7] |
| | | | | | | | | CCP2_3 | Capture of external signal(measure frequency or be used as external interrupts)、high-speed Pulse and Pulse-Width Modulation output channel-2 |
| P3.0/RxD/ $\overline{\text{INT4}}$ /T2CLKO | 18 | 24 | 21 | 17 | 13 | 15 | 11 | P3.0 | common I/O port PORT3[0] |
| | | | | | | | | RxD | Receive Data Port of UART1 |
| | | | | | | | | $\overline{\text{INT4}}$ | External interrupt 4, which only can be generated on falling edge. /INT4 supports power-down waking-up |
| | | | | | | | | T2CLKO | T2 Clock Output The pin can be configured for T2CLKO by setting INT_CLKO[2] bit /T2CLKO |
| P3.1/TxD/T2 | 19 | 25 | 22 | 18 | 14 | 16 | 12 | P3.1 | common I/O port PORT3[1] |
| | | | | | | | | TxD | Transit Data Port of UART1 |
| | | | | | | | | T2 | External input of Timer/Counter 2 |
| P3.2/INT0 | 20 | 26 | 23 | 19 | 15 | 17 | 13 | P3.2 | common I/O port PORT3[2] |
| | | | | | | | | INT0 | External interrupt 0, which both can be generated on rising and falling edge. INT0 only can generate interrupt on falling edge if IT0 (TCON.0) is set to 1. And, INT0 both can generate interrupt on rising and falling edge if IT0 (TCON.0) is set to 0. |
| P3.3/INT1 | 21 | 27 | 24 | 20 | 16 | 18 | 18 | P3.3 | common I/O port PORT3[3] |
| | | | | | | | | INT1 | External interrupt 1, which both can be generated on rising and falling edge. INT1 only can generate interrupt on falling edge if IT1 (TCON.2) is set to 1. And, INT1 both can generate interrupt on rising and falling edge if IT1 (TCON.2) is set to 0. INT1 supports power-down waking-up |
| P3.4/T0/ T1CLKO/ ECI_2 | 22 | 28 | 25 | 21 | 17 | 19 | 14 | P3.4 | common I/O port PORT3[4] |
| | | | | | | | | T0 | External input of Timer/Counter 0 |
| | | | | | | | | T1CLKO | T1 Clock Output The pin can be configured for T1CLKO by setting INT_CLKO[1] bit /T1CLKO |
| | | | | | | | | ECI_2 | External pulse input pin of CCP/PCA counter |
| P3.5/T1/ T0CLKO/ CCP0_2 | 23 | 29 | 26 | 22 | 18 | 20 | 15 | P3.5 | common I/O port PORT3[5] |
| | | | | | | | | T1 | External input of Timer/Counter 1 |
| | | | | | | | | T0CLKO | T0 Clock Output The pin can be configured for T0CLKO by setting INT_CLKO[0] bit /T0CLKO |
| | | | | | | | | CCP0_2 | Capture of external signal(measure frequency or be used as external interrupts)、high-speed Pulse and Pulse-Width Modulation output channel-0 |

| MNEMONIC | Pin Number | | | | | | | DESCRIPTION | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP44 | PLCC44 | PDIP40 | SOP32 | LQFP32 | SOP28 SKDIP28 | TSSOP20 | | |
| P3.6/$\overline{\text{INT2}}$ /RxD_2/ CCP1_2 | 24 | 30 | 27 | 23 | 19 | 21 | 16 | P3.6 | common I/O port PORT3[6] |
| | | | | | | | | $\overline{\text{INT2}}$ | External interrupt 2, which only can be generated on falling edge. /INT2 supports power-down waking-up |
| | | | | | | | | RxD_2 | Receive Data Port of UART1 |
| | | | | | | | | CCP1_2 | Capture of external signal(measure frequency or be used as external interrupts)、high-speed Pulse and Pulse-Width Modulation output channel-1 |
| P3.7/$\overline{\text{INT3}}$ /TxD_2/CCP2/ CCP2_2 | 25 | 31 | 28 | 24 | 20 | 22 | 17 | P3.7 | common I/O port PORT3[7] |
| | | | | | | | | $\overline{\text{INT3}}$ | External interrupt 3, which only can be generated on falling edge. /INT3 supports power-down waking-up |
| | | | | | | | | TxD_2 | Transit Data Port of UART1 |
| | | | | | | | | CCP2 | Capture of external signal(measure frequency or be used as external interrupts)、high-speed Pulse and Pulse-Width Modulation output channel-2 |
| | | | | | | | | CCP2_2 | Capture of external signal(measure frequency or be used as external interrupts)、high-speed Pulse and Pulse-Width Modulation output channel-2 |
| P4.0/MOSI_3 | 17 | 23 | - | - | - | - | | P4.0 | common I/O port PORT4[0] |
| | | | | | | | | MISO_3 | Master Iutput Slave Onput of SPI |
| P4.1/MISO_3 | 26 | 32 | 29 | - | - | - | | P4.1 | common I/O port PORT4[1] |
| | | | | | | | | MOSI_3 | Master Output Slave Input of SPI |
| P4.2/$\overline{\text{WR}}$ | 27 | 33 | 30 | - | - | - | | P4.2 | common I/O port PORT4[2] |
| | | | | | | | | $\overline{\text{WR}}$ | Write pulse of external data memory |
| P4.3/SCLK_3 | 28 | 34 | - | - | - | - | | P4.3 | PORT4[3] |
| | | | | | | | | SCLK_3 | Clock Signal of synchronous serial peripheral interface----SPI |
| P4.4/$\overline{\text{RD}}$ | 29 | 35 | 31 | - | - | - | | P4.4 | common I/O port PORT4[4] |
| | | | | | | | | $\overline{\text{RD}}$ | Read pulse of external data memory |
| P4.5/ALE | 38 | 44 | 40 | - | - | - | | P4.5 | common I/O port PORT4[5] |
| | | | | | | | | ALE | Address Latch Enable. It is used for external data memory cycles (MOVX) |
| P4.6/RxD2_2 | 39 | 1 | - | - | - | - | | P4.6 | common I/O port PORT4[6] |
| | | | | | | | | RxD2_2 | Receive Data Port of UART2 |
| P4.7/TxD2_2 | 6 | 12 | - | - | - | - | | P4.7 | common I/O port PORT4[7] |
| | | | | | | | | TxD2_2 | Transit Data Port of UART2 |

| MNEMONIC | Pin Number | | | | | | | DESCRIPTION | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP44 | PLCC44 | PDIP40 | SOP32 | LQFP32 | SOP28 SKDIP28 | TSSOP20 | | |
| P5.4/RST/ MCLKO/SS_3 | 13 | 19 | 17 | 13 | 9 | 11 | 7 | P5.4 | common I/O port PORT5[4] |
| | | | | | | | | RST | Reset pin. A high on this pin for at least two machine cycles will reset the device. |
| | | | | | | | | MCLKO | Master clock output; the output frequency can be MCLK/1, MCLK/2 and MCLK/4. The master clock can either be internal R/C clock or the external input clock or the external crystal oscillator. |
| | | | | | | | | SS_3 | Slave selection signal of synchronous serial peripheral interface----SPI |
| P5.5 | 15 | 21 | 19 | 15 | 11 | 13 | 9 | common I/O port PORT5[5] | |
| Vcc | 14 | 20 | 18 | 14 | 10 | 12 | 8 | The positive pole of power | |
| Gnd | 16 | 22 | 20 | 16 | 12 | 14 | 10 | The negative pole of power, Gound | |